SERVICE MANUAL

A500

OCTOBER, 1990 PN-314981-04

Commodore

Produced By:

Commodore International Spare Parts GmbH
Braunschweig, West Germany

SERVICE MANUAL

A500

OCTOBER, 1990 **PN-314981-04**

INTERNATIONAL EDITION

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SECTION 1

SPECIFICATIONS

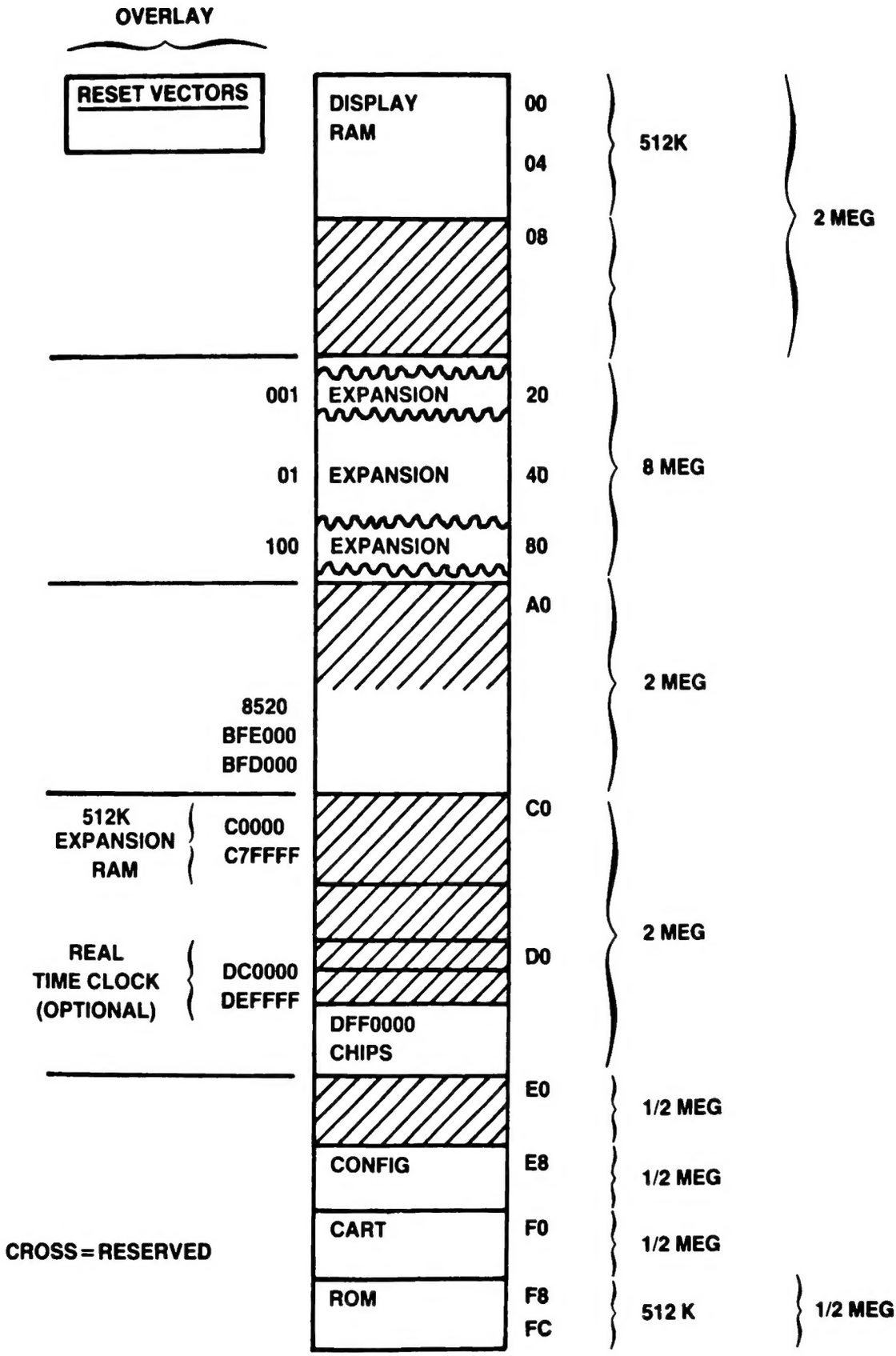
Amiga A500 Specifications

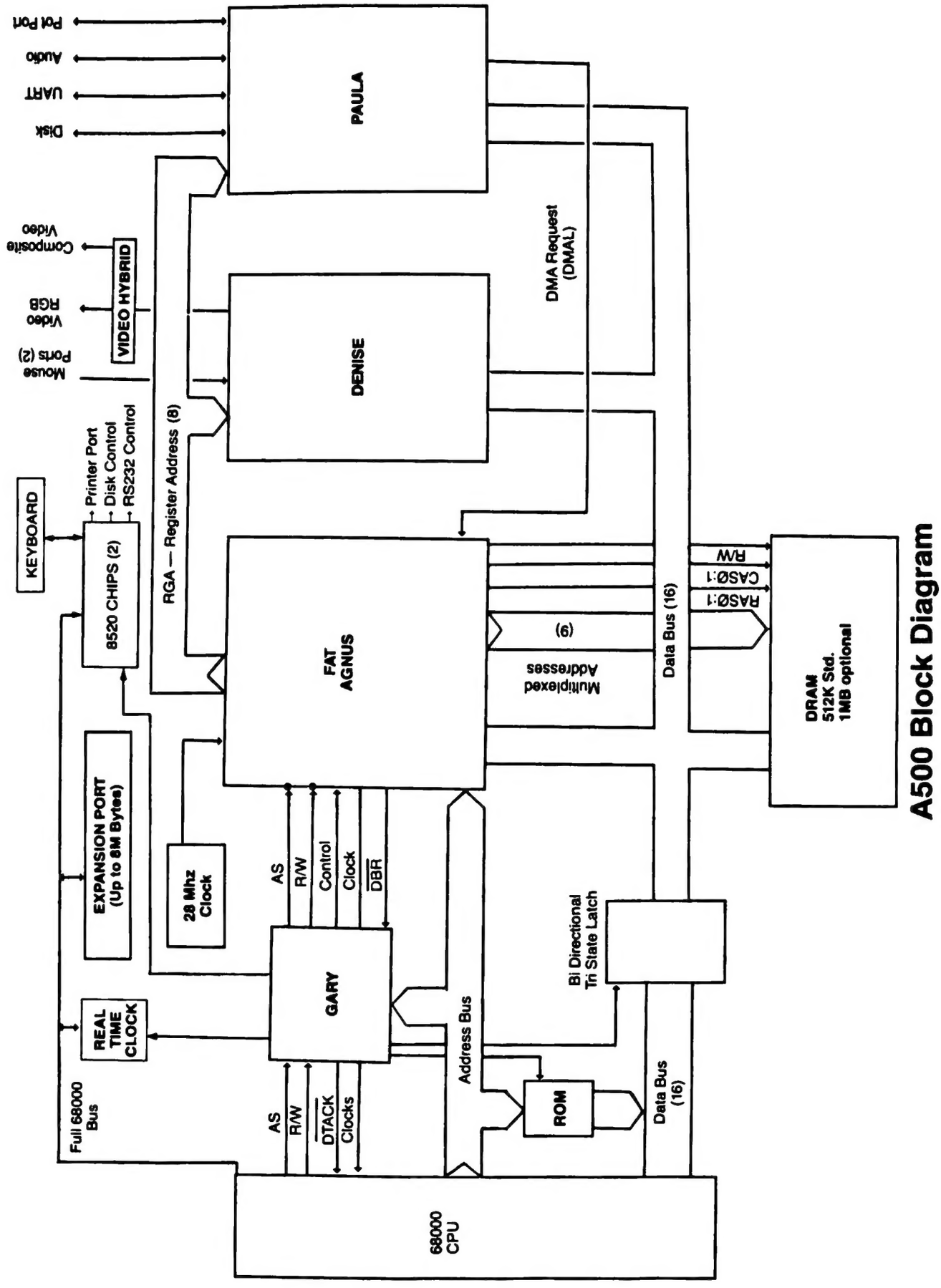
Central Processor	Motorola MC68000
Memory	512K bytes RAM expandable to 1M
Disks	3-1/2 inch double-sided double-density microdisks with 880K bytes formatted storage capacity per disk
Mouse	Mechanical, .13 mm/count (200 counts per inch)
Interfaces	RS-232 serial interface Centronics®-compatible parallel interface External disk interface Mouse/Game controller interface Additional game controller interface Keyboard interface Two audio outputs for stereo sound Memory cartridge interface Expansion interface
Supported Monitors	Analog RGB, digital RGB, monochrome (composite video), and standard televisions
Power Requirements	99 to 121 volts AC 54 to 66 Hz
Temperature Requirements	For operation: 5 to 40 degrees Centigrade (41 to 104 degrees Fahrenheit) For storage: -40 to 60 degrees Centigrade (-40 to 140 degrees Fahrenheit)
Humidity Requirements	20% to 90% relative humidity, non-condensing

SECTION 2

THEORY OF OPERATIONS

Amiga 500 Memory Map





A500 Block Diagram

Theory of Operation

The AMIGA computer is a high-performance system with advanced graphics and audio features. The principal hardware features consist of the 68000 microprocessor which runs at 7.2 MHz, 512K RAM, expandable to 1MB, and configurable to 8MB, 2 parallel I/O chips, one control chip (GARY) and 3 custom VLSI chips that provide the unique capabilities for animation, graphics and sound.

68000 Microprocessor

The 68000 is the CPU of the system. All other resources are under software control via control data issued from it. All 3 custom chips have control registers that are written by the 68000.

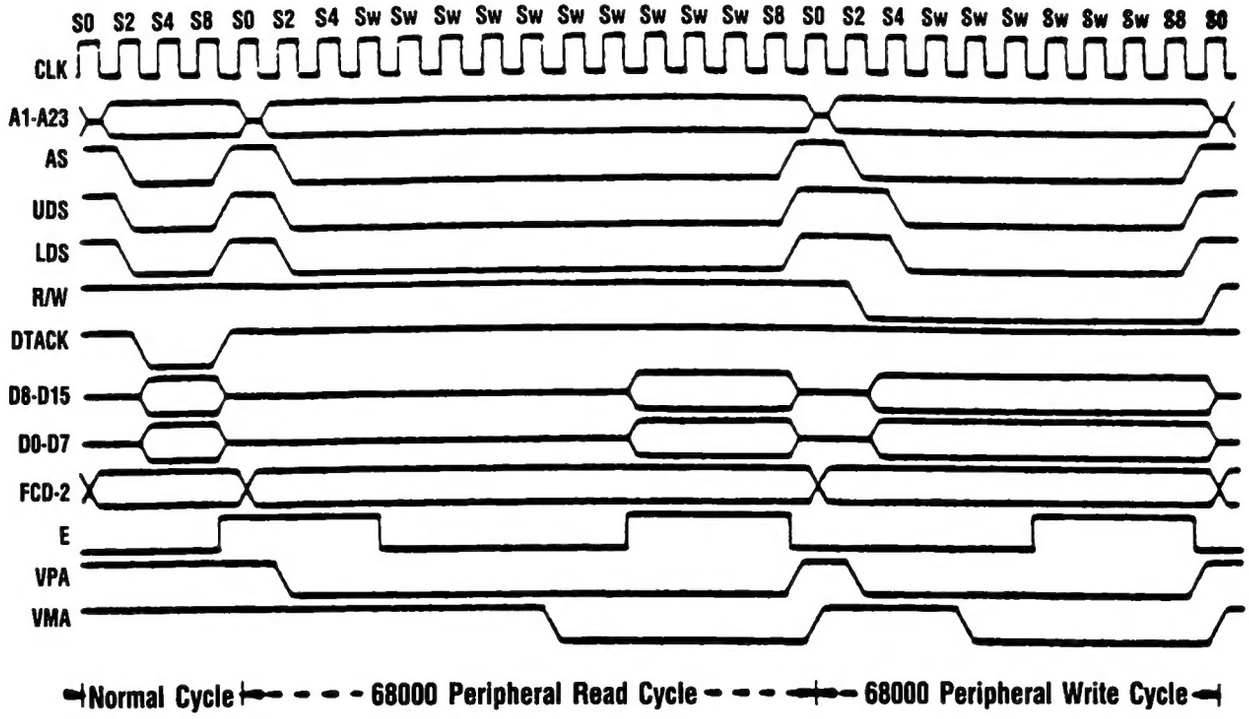
The 68000 communicates with the rest of the computer via its address bus, data bus and control lines. Notice that in the block diagram the 3 custom chips do not reside directly on the 68000 buses. When the 68000 starts a bus cycle that is intended for the custom chips or the display RAM, the bus control chip detects whether or not the display RAM buses are available. The control chip will not assert the acknowledge signal (/DTACK) back to the 68000 until the display RAM buses are available. Once the 68000 receives /DTACK it completes the bus cycle. Connecting the display RAM buses to the 68000 buses is discussed further in the section on bus control. Because the display RAM is capable of approximately twice the bandwidth of the 68000, the 68000 is usually not delayed by waiting for the display buses to become available.

The 68000 can fetch instructions from:

Display RAM
ROM

The 68000 can read and write data directly to:

Display RAM
Parallel I/O Chips
3 Custom I.C.s
ROM



CPU Machine Cycle

SIGNAL SUMMARY

Signal Name	Mnemonic	Input/Output	Active State	Three State
Address Bus	A1-A23	Output	High	Yes
Data Bus	D0-D15	Input/Output	High	Yes
Address Strobe	$\overline{AS}$	Output	Low	Yes
Read/Write	R/$\overline{W}$	Output	Read-High Write-Low	Yes
Upper and Lower Data Strobes	$\overline{UDS}$, $\overline{LDS}$	Output	Low	Yes
Data Transfer Acknowledge	$\overline{DTACK}$	Input	Low	No
Bus Request	$\overline{BR}$	Input	Low	No
Bus Grant	$\overline{BG}$	Output	Low	No
Bus Grant Acknowledge	$\overline{BGACK}$	Input	Low	No
Interrupt Priority Level	$\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$	Input	Low	No
Bus Error	$\overline{BERR}$	Input	Low	No
Reset	$\overline{RESET}$	Input/Output	Low	No*
Halt	$\overline{HALT}$	Input/Output	Low	No*
Enable	E	Output	High	No
Valid Memory Address	$\overline{VMA}$	Output	Low	Yes
Valid Peripheral Address	$\overline{VPA}$	Input	Low	No
Function Code Output	FC0, FC1, FC2	Output	High	Yes
Clock	CLK	Input	High	No
Power Input	Vcc	Input	—	—
Ground	GND	Input	—	—

*Open Drain

A0 is internal to 68000

The 68000 transmits data and control to and from the peripherals via the parallel I/O and the 3 custom chips.

7M is the processor clock to the 68000. C1, C3 and CDAC are used to clock the custom chips and determine the timing of signals to the memory arrays.

ROM

The ROM contains the kernel and DOS routines; it is 128K × 16.

Parallel I/O

The 2 multipurpose 8520 I/O chips provide the following:

I/O to and from the parallel port connector
Control lines to and from the joystick/mouse ports
A control line to the front panel LED
Internal control lines
Keyboard control lines, clock and data
Serial port control lines
Floppy disk interface control lines
Internal timers

These 2 chips reside on the 68000 buses and are read and written by the 68000.

Clocks Generator

The entire computer board is run synchronously to the 3.57954Mhz color clock (C1). This is accomplished by generating a number of sub-multiple frequencies from our master 28.63636Mhz crystal oscillator. The following are the primary clocks on the board:

Name	Description
C1	The 3.579545Mhz Color Clock
C2	C1 shifted 45 degrees later
C3	C1 shifted 90 degrees later
C4	C1 shifted 135 degrees later
7M	C1 XORed with C3* (7.15909Mhz)
DAC	7M shifted 90 degrees later

7M is the processor clock for the 68000 microprocessor. C1-C4 and DAC are used to clock the custom chips and for determining the timing of signals to the memory arrays.

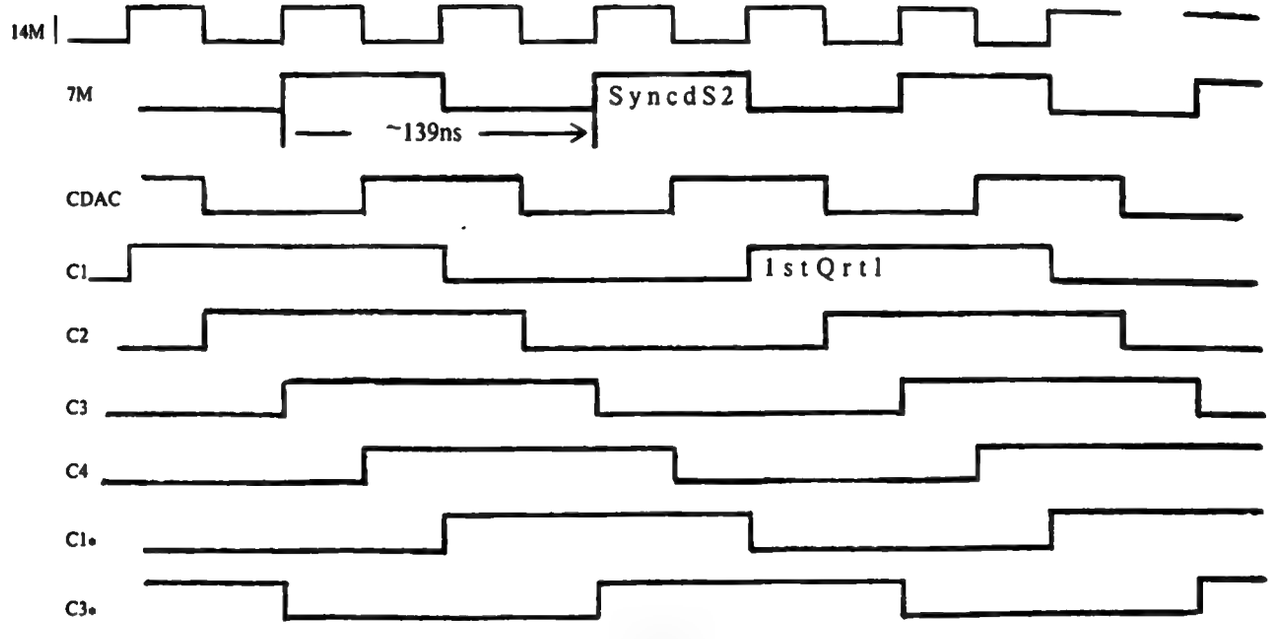
The above frequencies are true for NTSC Amigas. A PAL Amiga will operate slightly slower, with a main clock of 28.37516Mhz. This is divided down to get 7M = 7.09379Mhz and C1 = 3.546895Mhz. A special circuit is required to take five fourths of C1 to derive the PAL colorburst frequency of 4.43361875Mhz.

The following clocks are available at the edge connector:

Name	Pin	Description
C3*	14	C3 inverted
CDAC	15	DAC equivalent
C1*	16	C1 inverted

Note that 7M (the processor clock) is not available at the connector; it can be easily generated by:
C3* XNOR C1* = 7M equivalent

If you need a 14.31818Mhz synchronous clock, you can generate it by:
(7Mequiv) XOR (CDAC) = 14M equivalent



Amiga System Clocks

The 3 Custom Chips

The 3 custom chips provide very fast manipulation of graphics and audio data in the display RAM. All the major functions in the chips are DMA driven; that is, streams of data are moved between the custom chips and display RAM under DMA control. These streams of data are acted upon by the custom chips. Fat Agnus, custom chip #1, contains 25 dedicated purpose DMA counters.

The 3 chips have control registers which are usually loaded by the 68000. However, Fat Agnus also has the capability of loading control registers in the other 2 custom chips. When Fat Agnus performs a bus cycle, it outputs a code on the Register Address Bus telling the other 2 chips the nature of the bus cycle. This is necessary because many of the bus cycles provide data to or from the other 2 chips, thus they must cooperate appropriately.

In addition to manipulating data in the display RAM, the custom chips output streams of data to the video output circuits and audio output circuits, and they move data to and from the floppy disks and serial port.

Note that the display RAM buses can be completely isolated from the 68000 buses by Fat Agnus and Data Bus drivers. Thus, Fat Agnus can be performing a bus cycle on the display buses simultaneously with the 68000 performing a bus cycle on its buses. This parallelism increases throughout.

Bus Control, Address/Data MUX, Address Driver

The bus control logic resides in the control chip (GARY) and Fat Agnus. They provide 3 major functions, they:

Synchronize the 68000 to the current phase of C1
Arbitrate between the 68000 and Fat Agnus for the display buses
Generate DRAM timing for the video RAM bus drivers appropriate to the current cycle

Synchronizing the 68000 to C1 is straightforward, since the 68000 is clocked by 7M which is twice the frequency and synchronous to C1. If the 68000 starts a bus cycle in the wrong phase of C1, the bus control chip merely delays /DTACK long enough so that the 68000 will complete the bus cycle in the desired phase relationship to C1. This phase relationship is necessary because the custom chips and the display RAM are clocked by C1.

Arbitration is very simple. Fat Agnus tells the bus control prior to taking the display RAM buses by asserting an input to the control chip (GARY) called / DBR. Whenever Fat Agnus has the display buses and the 68000 wants them, the 68000 is held off by not giving it /DTACK. In this state the 68000 has no effect on the display buses until the bus controller enables the bus drivers.

Fat Agnus generates the DRAM timings and does all address multiplexing. If the 68000 is running a video memory cycle, its addresses are routed through Fat Agnus onto the multiplexed address lines. If the custom chips are running a memory cycle the addresses are routed to the multiplexed address lines from internal address register.

Display RAM

The display RAM is a 512K read/write memory that resides on the RAM address and RAM data buses. It is expandable to 1M bytes by the addition of the RAM expansion module. It is implemented using standard 256K × 1 dynamic RAMs, refreshed by Fat Agnus.

The display RAM is really used for much more than just holding graphics data. It also stores code and data for the 68000.

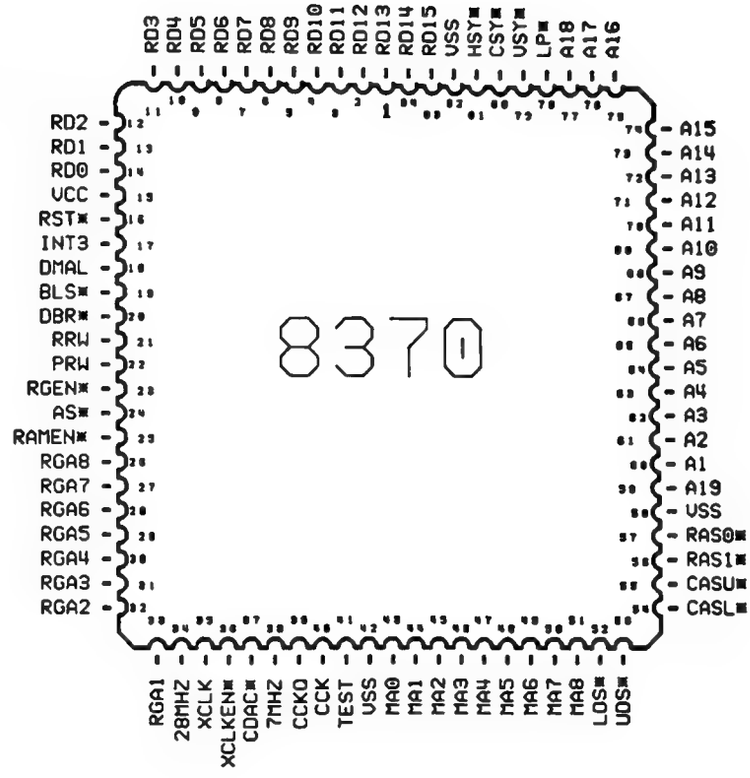
Custom Control Chips

The Amiga's animation, graphics and sound are produced by three custom chips. Fat Agnus (8370), Denise (8362) and Paula (8364). A fourth custom chip, Gary serves as the control chip. The following pages include pin diagrams, feature lists, and block diagrams for these chips.

Custom Animation Chip
Fat Agnus

Features:

- Bit Blitter — Uses hardware to move display data — Allows high speed animation — Frees the CPU for other concurrent tasks
- Display Synchronized Coprocessor
- Controls 25 DMA Channels — Allows the disk and sound to operate with minimal CPU intervention
- Generates all system clocks from the 28 Mhz oscillator
- Generates all control signals for the video RAM and expansion RAM card
- Provides the address to the video and expansion RAM multiplexing



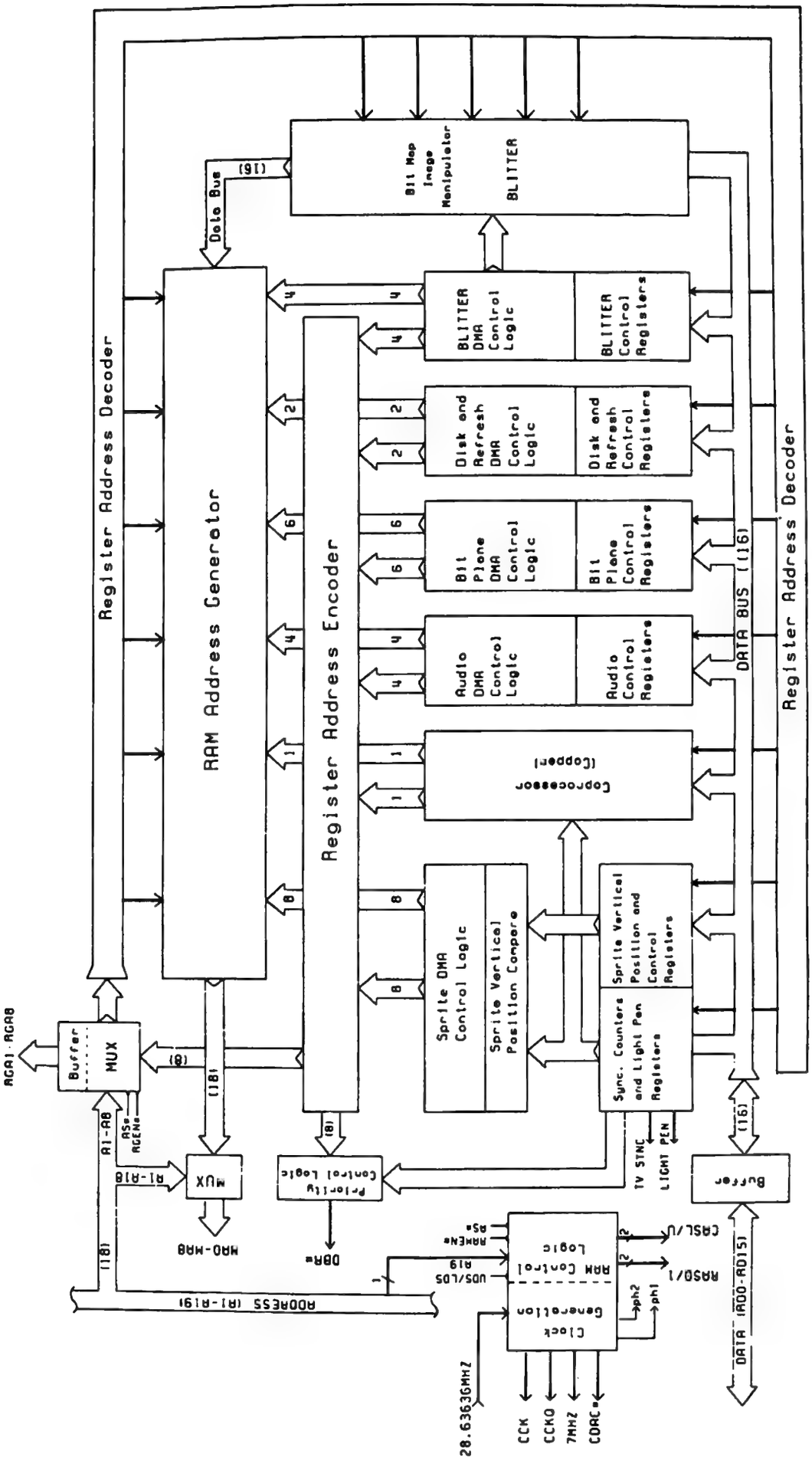
One Megabyte Agnus use in Commodore A500 Computers.

Commodore Business Machines does not support the One Megabyte addressing feature of the Fat Agnus 8372 IC in A500 Computers.

Regardless of the version of Fat Agnus, all A500's have been factory jumper set to be functionally identical.

8370 Fat Agnus chips are used on rev 5 boards with 256K x 1 DRAMS. 8372 Fat Agnus chips are used on rev 6a boards with 256K x 4 DRAMS. The boards are functionally interchangable. Each will support 512K of chip RAM and 512K of expansion RAM with an A501 installed.

Enabling the One Megabyte feature, at the customers' request, will void the warranty. Instructions detailing implementation of the One Megabyte addressing have been circulated without Official Approval and Commodore does not assume any liability for damages resulting from this mode of operation in the A500.

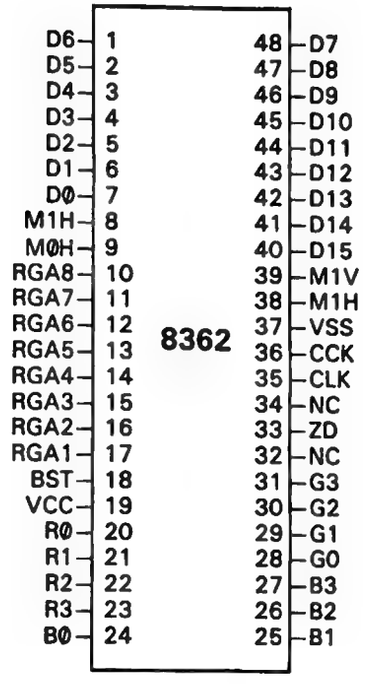


Fat Agnus Block Diagram

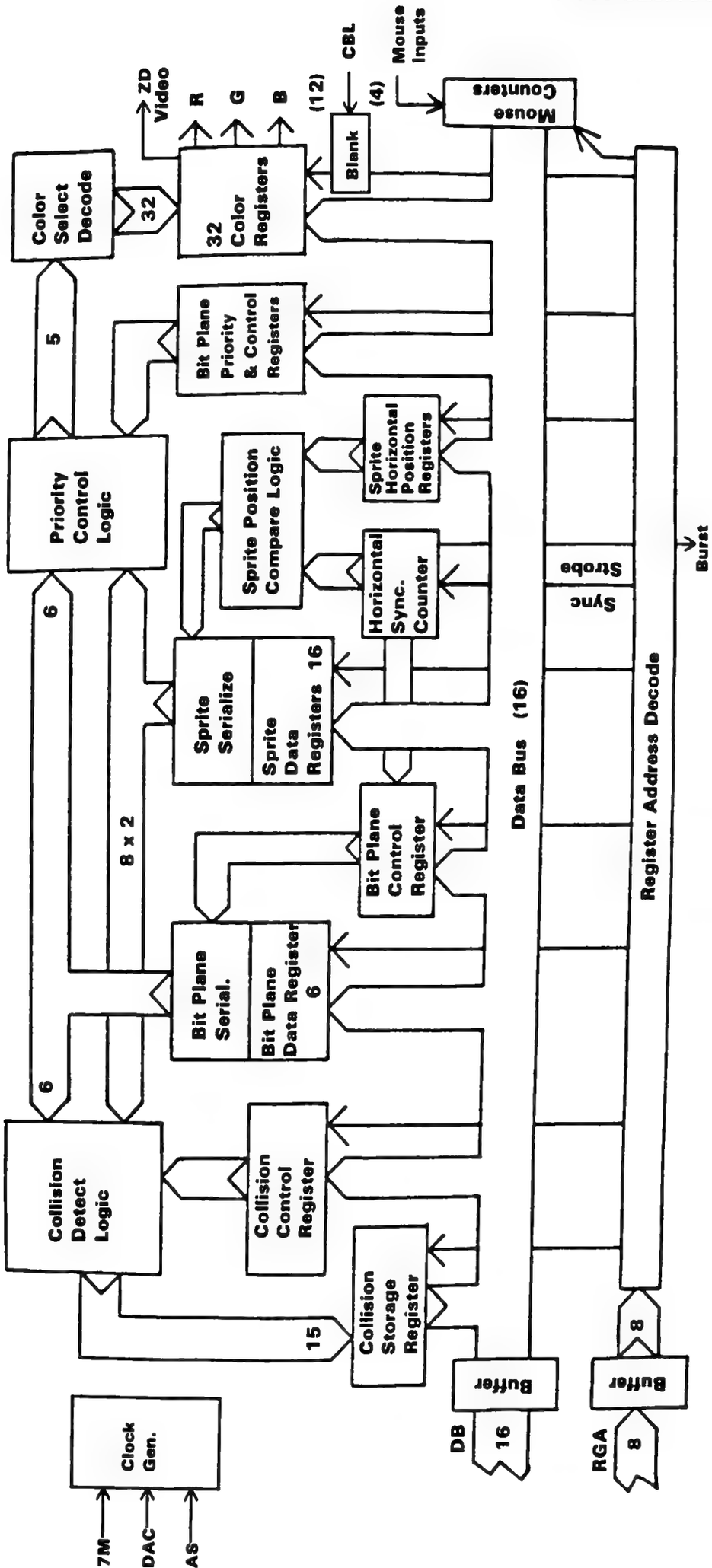
Custom Graphics Chip
Denise

Features:

- Many different resolutions
  320 × 200 up to 640 × 400
- 4096 colors on a TV or RGB monitor
- Eight re-usable sprite controllers
- 60 or 80 column text
- Same software for all TVs and monitors



Pin	Name	Description	Type
1-7	D0-D6	Data Bus Lines 0-6	I/O
8	M1H	Mouse 1 Horizontal	I
9	M0H	Mouse 0 Horizontal	I
10-17	RGA1-8	Register Address 1-8	I
18	/BURST	Color Burst	O
19	Vcc	+5 VDC	I
20-23	R0-3	Video Red Bit 0-3	O
24-27	B0-3	Video Blue Bit 0-3	O
28-31	G0-3	Video Green Bit 0-3	O
32	N/C	No Connection	N/C
33	/ZD	Background Indicator	O
34	N/C	No Connection	N/C
35	7M	7.15909 MHz Clock	I
36	CCK	Color Clock	I
37	Vss	Ground	I
38	M0V	Mouse 0 Vertical	I
39	M1V	Mouse 1 Vertical	I
40-48	D7-D15	Data Bus Lines 7-15	I/O

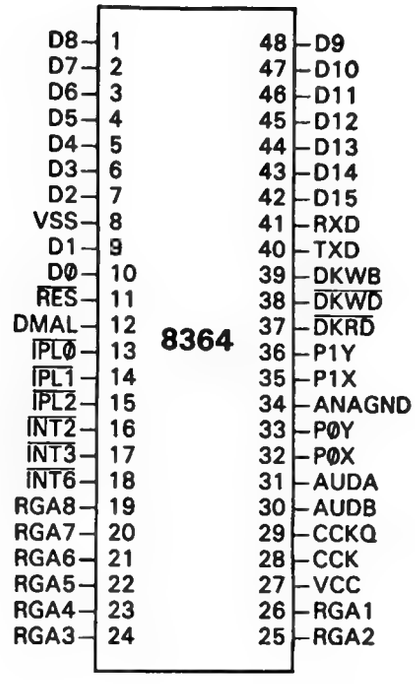


Denise Block Diagram

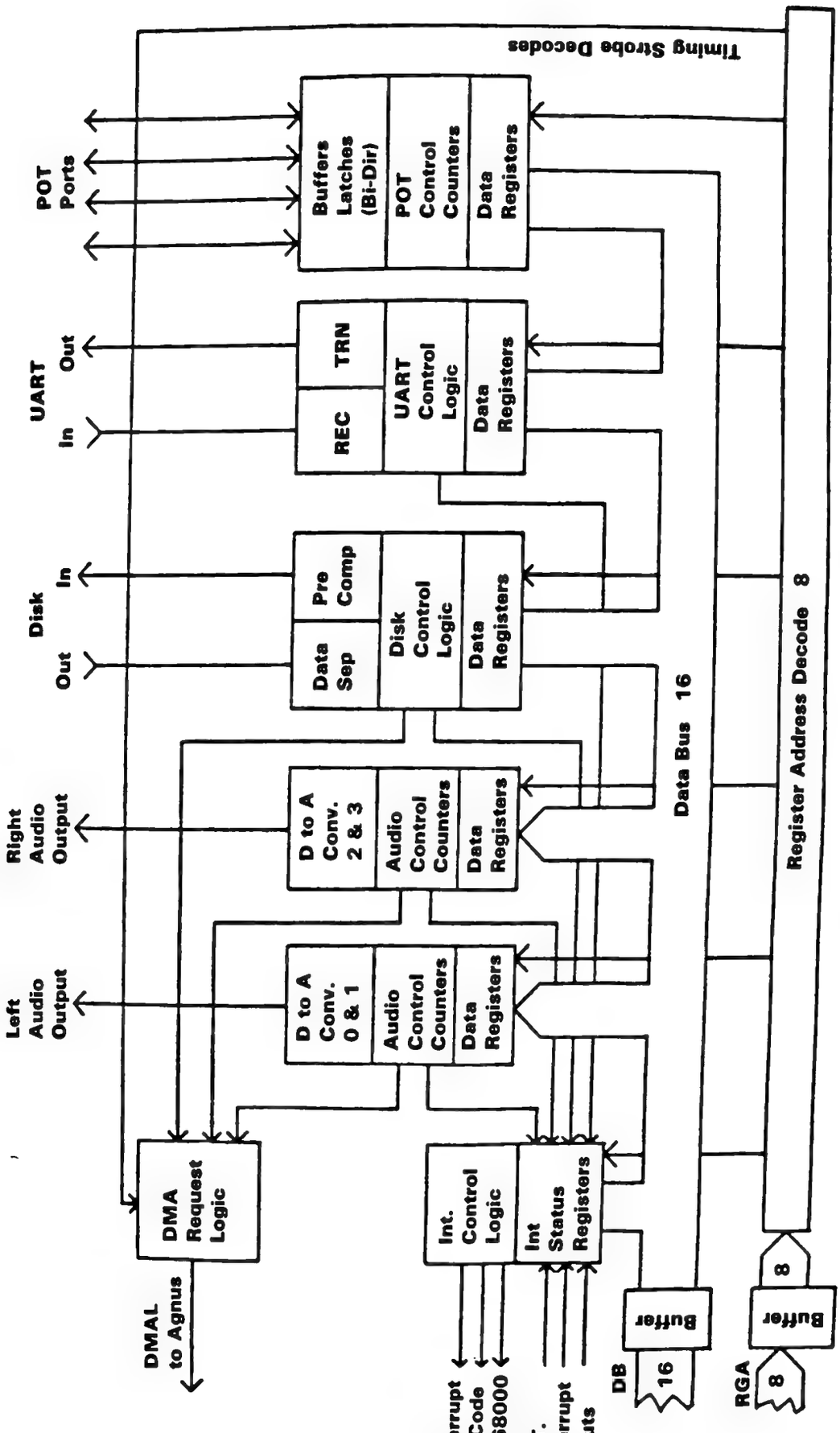
Custom Sound/Peripherals Chip
Paula

Features:

- Four voices of sound output configured as two stereo channels
- Nine octaves
- Complex waveforms
- Uses both amplitude and frequency modulation
- I/O controls for disk data and controller ports
- Microdisk controller
- Interrupt control system



Pin	Name	Description	Type
1-7	D2-D8	Data Bus Lines 2-8	I/O
8	Vss	Ground	I
9,10	D0,D1	Data Bus Lines 0,1	I/O
11	/RES	System Reset	I
12	DMAL	DMA Request Line	O
13-15	/IPL0-2	Interrupt Line 0-2	O
16-18	/INT2,3,6	Interrupt Level 2,3,6	I
19-26	RGA1-8	Register Address 1-8	I
27	Vcc	+5 VDC	I
28	CCK	Color Clock	I
29	CCKQ	Color Clock Delay	I
30	AUDB	Right Audio	O
31	AUDA	Left Audio	O
32	POT0X	Pot 0X	I/O
33	POT0Y	Pot 0Y	I/O
34	VSSANA	Analog Ground	I
35	POT1X	Pot 1X	I/O
36	POT1Y	Pot 1Y	I/O
37	/DKRD	Disk Read Data	I
38	/DKWD	Disk Write Data	O
39	DKWE	Disk Write Enable	O
40	TXD	Serial Transmit Data	O
41	RXD	Serial Receive Data	I
42-48	D9-15	Data Bus Lines 9-15	I/O

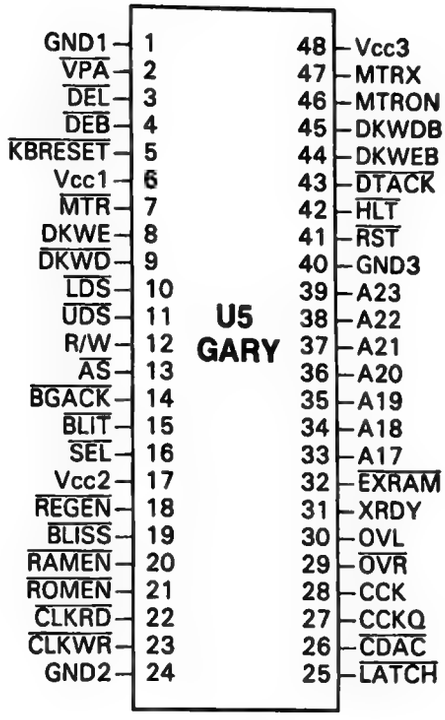


Paula Block Diagram

Custom Control Chip
Gary

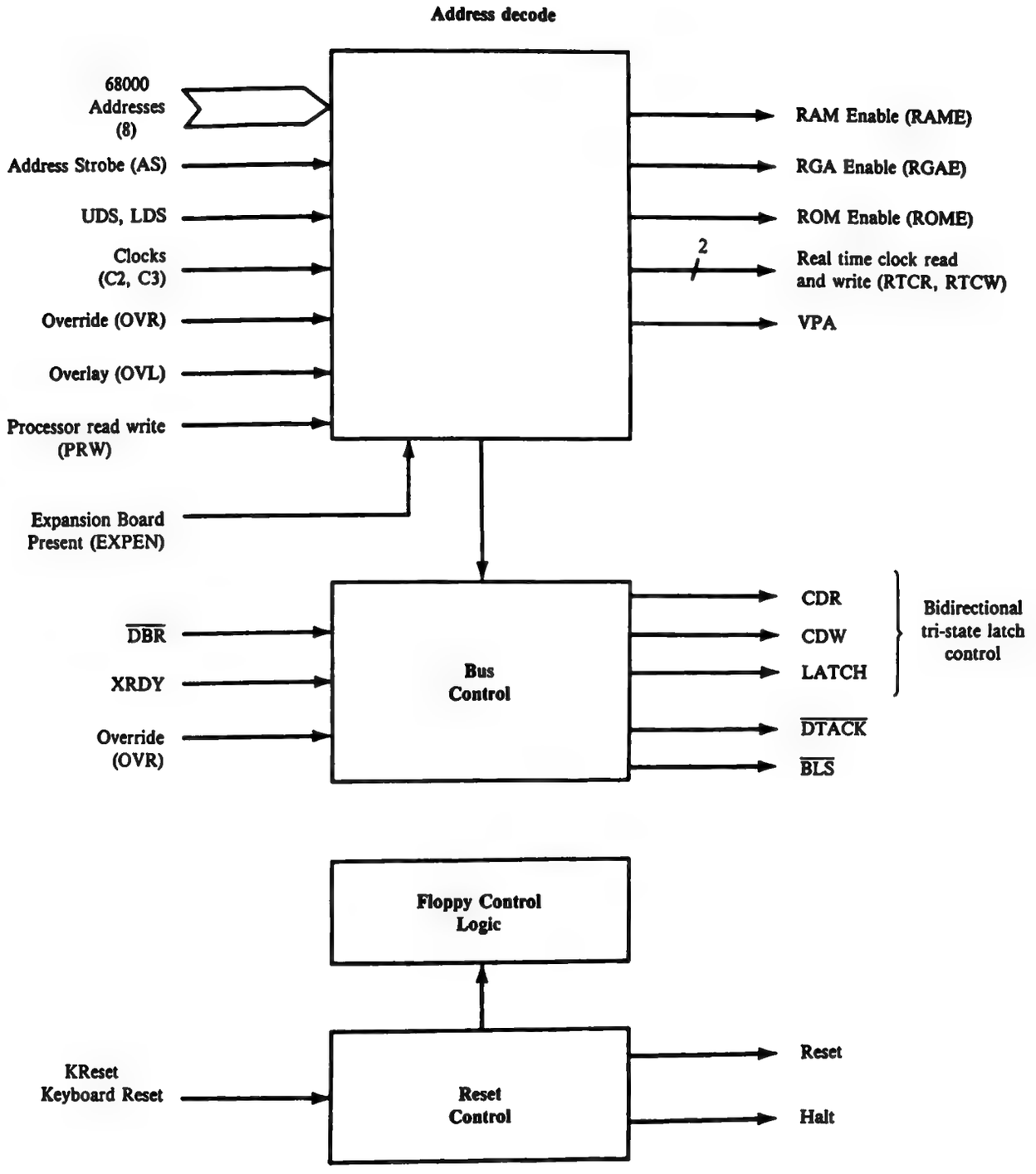
Features:

- Provides all bus control signals.
- Provides all address decoding.
- Generates the 68000 VPA signal.
- Handles some of the floppy circuitry.
- Provides keyboard reset interface.

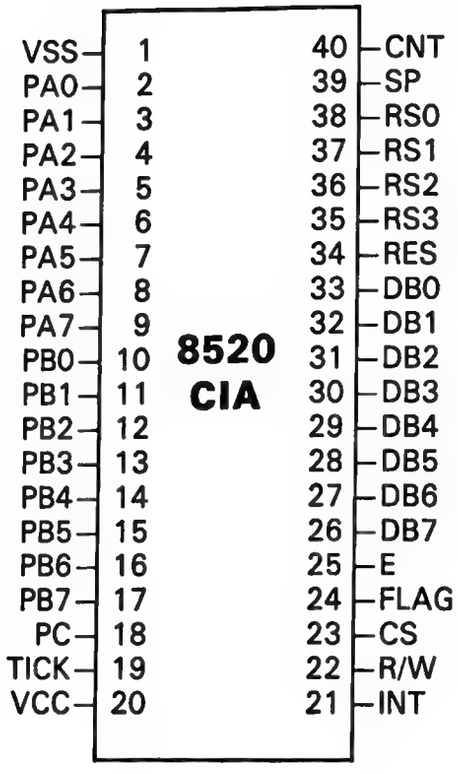


For signal descriptions see Schematic #312511 (sheet 1 of 9)

Gary Block Diagram



Complex Interface Adapter



INTERFACE SIGNALS

E Clock Input

Peripheral Clock from 68000 (10 cycles of 7.16Mhz clock — 6 high, 4 low)

CS — Chip Select Input

The CS input controls the activity of the 8520. A low level on CS while 02 is high causes the device to respond to signals on the R/W and address (RS) lines. A high on CS prevents these lines from controlling the 8520. The CS line is normally activated (low) at 02 by the appropriate address combination.

R/W — Read/Write Input

The R/W signal is normally supplied by the microprocessor and controls the direction of data transfers of the 8520. A high on R/W indicates a read (data transfer out of the 8520), while a low indicates a write (data transfer into the 8520).

RS3-RS0 — Address Inputs

The address inputs select the internal registers as described by the Register Map.

DB7-DB0 — Data Bus Inputs/ Outputs

The eight bit data bus transfers information between the 8520 and the system data bus. These pins are high impedance inputs unless CS is low and R/W and 02 are high, to read the device. During this read, the data bus output buffers are enabled, driving the data from the selected register onto the system data bus.

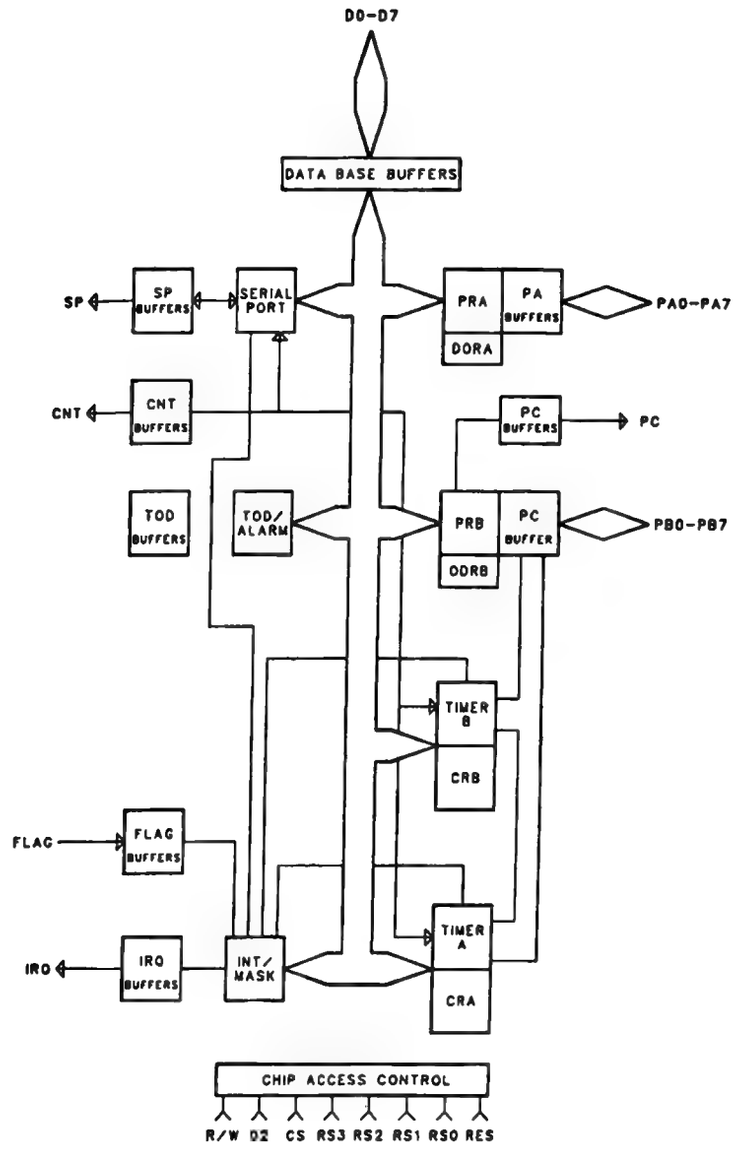
INT — (IRQ) Interrupt Request Output

IRQ is an open drain output normally connected to the processor interrupt input. An external pullup resistor holds the signal high, allowing multiple IRQ-outputs to be connected together. The IRQ output is normally off (high impedance) and is activated low as indicated in the functional description.

RES — Reset Input

A low on the RES pin resets all internal registers. The port pins are set as inputs and port registers to zero (although a read of the ports will return all highs because of passive pullups). The timer control registers are set to zero and the timer latches to all ones. All other registers are reset to zero.

REGISTER MAP



RS3	RS2	RS1	RS0	REG		
0	0	0	0	0	PRA	Peripheral Data Reg. A
0	0	0	1	1	PRB	Peripheral Data Reg. B
0	0	1	0	2	DDRA	Data Direction Reg. A
0	0	1	1	3	DDRB	Data Direction Reg. B
0	1	0	0	4	TA LO	Timer A Low Register
0	1	0	1	5	TA HI	Timer A High Register
0	1	1	0	6	TB LO	Timer B Low Register
0	1	1	1	7	TB HI	Timer B High Register
1	0	0	0	8		Event LSB
1	0	0	1	9		Event 8-15
1	0	1	0	A		Event MSB
1	0	1	1	B		No Connect
1	1	0	0	C	SDR	Serial Data Register
1	1	0	1	D	ICR	Interrupt Control Register
1	1	1	0	E	CRA	Control Register A
1	1	1	1	F	CRB	Control Register B

FUNCTION DESCRIPTION

I/O Ports (PRA, PRB, DDRA, DDRB)

Ports A and B each consist of an 8-bit Peripheral Data Register (PR) and an 8-bit Data Direction Register (DDR). If a bit in the DDR is set to the corresponding bit in the PR it is an output. If a DDR bit is set to zero, the corresponding PR bit is defined an an input. On a READ, the PR reflects the information present on the actual port pins (PA0-PA7, PBO-PB7) for both input and output bits. Port A has both passive and active pullup devices, providing both CMOS and TTL compatibility. It can drive 2 TTL loads. Port B has only passive pullup device and has a much higher current-sinking capability.

Handshaking

Handshaking on data transfers can be accomplished using the PC output pin and the FLAG input pin. PC will go low on the 3rd cycle after a PORT B access. This signal can be used to indicate "data ready" at PORT B or "data accepted" from PORT B. Handshaking on a 16-bit data transfers (using both PORT A and PORT B) is possible by always reading or writing PORT A first. FLAG is a negative edge sensitive input which can be used for receiving the PC output from another 8520 or as a general purpose interrupt input. Any negative transition on FLAG will set the FLAG interrupt bit.

Reg	Name	D7	D6	D5	D4	D3	D2	D1	D0
0	PRA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
1	PPB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
2	DDRA	DPA7	DPA6	DPA5	DPA4	DPA3	DPA2	DPA1	DPA0
3	DDRB	DPB7	DPB6	DPB5	DPB4	DPB3	DPB2	DPB1	DPB0

Interval Timers (Timer A, Timer B)

Each interval timer consists of a 16-bit read-only Timer Counter and a 16-bit write-only Timer Latch. Data written to the timer is latched in the Timer Latch, while data read from the timer are the present contents of the Timer Counter. The timers can be used independently or linked for extended operations. The various timer modes allow generation of long time delays, variable width pulses, pulse trains and variable frequency waveforms. Utilizing the CNT input, the timers can count external pulses or measure frequency, pulse width and delay times of external signals. Each timer has an associated control register, providing independent control of the following functions.

Start/Stop

A control bit allows the timer to be started or stopped by the microprocessor at any time.

PB On/Off

A control bit allows the timer output to appear on a PORT B output line (PB6 for TIMER A and PB7 for TIMER B). This function overrides the DDRB control bit and forces the appropriate PB line to an output.

Toggle/Pulse

A control bit selects the output applied to PORT B. On every timer underflow the output can either toggle or generate a single positive pulse of one cycle duration. The toggle output is set high whenever the timer is started and is set low by RES.

One-Shot/Continuous

A control bit selects either timer mode. In one-shot mode, the timer will count down form the latched value to zero, generate an interrupt, reload the latched value, then stop. In continuous mode, the timer will count from the latched value to zero, generate an interrupt, reload the latched value and repeat the procedure continuously. In one-shot mode: a write to Timer High (registers 5 for TIMER A, 7 for TIMER B) will transfer the timer latch to the counter and inititate counting regardless of the start bit.

Force Load

A strobe bit allows the timer latch to be loaded into the timer counter at any time, whether the timer is running or not.

Input Mode

Control bits allow selection of the clock used to decrement the timer. TIMER A can count 02 pulses or external pulses applied to the CNT pin. TIMER B can count 02 pulses, external CNT pulses, TIMER A underflow pulses or TIMER A underflow pulses while the CNT pin is held high.

The timer latch is loaded into the timer on any timer underflow, on a force load or following a write to the high byte of the prescaler while the timer is stopped. If the timer is running, a write to the high byte will load the timer latch, but not reload the counter.

READ (TIMER)

REG	Name								
4	TA LO	TAL7	TAL6	TAL5	TAL4	TAL3	TAL2	TAL1	TAL0
5	TA HI	TAH7	TAH6	TAH5	TAH4	TAH3	TAH2	TAH1	TAH0
6	TB LO	TBL7	TBL6	TBL5	TBL4	TBL3	TBL2	TBL1	TBL0
7	TB HI	TBH7	TBH6	TBH5	TBH4	TBH3	TBH2	TBH1	TBH0

WRITE (PRESCALER)

REG	Name								
4	TA LO	PAL7	PAL6	PAL5	PAL4	PAL3	PAL2	PAL1	PAL0
5	TA HI	PAH7	PAH6	PAH5	PAH4	PAH3	PAH2	PAH1	PAH0
6	TB LO	PBL7	PBL6	PBL5	PBL4	PBL3	PBL2	PBL1	PBL0
7	TB HI	PBH7	PBH6	PBH5	PBH4	PBH3	PBH2	PBH1	PBH0

TOD (TICK)

TOD consists of a 24 bit binary counter. Positive edge transitions on this pin cause the binary counter to increment. The TOD pin has a passive pull-up on it. A programmable ALARM is provide for generating an interrupt at a desired time. The ALARM registers are located at the same addresses as the corresponding TOD register. Access to the ALARM is governed by a Control Register bit. The ALARM is write-only; any read of a TOD address will read time regardless of the state of the ALARM access bi:

A specific sequence of events must be followed for proper setting and reading of TOD. TOD is automatically stopped whenever a write to the register occurs. The clock will not start again until after a write to the LSB Event Register. This assures TOD will always start at the desired time. Since a carry from one stage to the next can occur at any time with respect to a read operation, a latching function is include to keep all Time of Day information constant during a read sequence. All TOD registers latch on a read of MSB event and remain latched until after a read of LSB Event. The TOD clock continues to count when the output registers are latched. If only one register is to be read, there is no carry problem and the register can be read "on the fly", provided that any read of MSB Event is followed by a read of LSB Event to disable the latching.

READ

REG	Name								
8	LSB Event	E7	E6	E5	E4	E3	E2	E1	E0
9	Event 8-15	E15	E14	E13	E12	E11	E10	E9	E8
A	MSB Event	E23	E22	E21	E20	E19	E18	E17	E16

WRITE
CRB7 = 0
CRB7 = 1 ALARM
(SAME FORMAT AS READ)

Serial Port (SDR)

The serial port is a buffered, 8-bit synchronous shift register system. A control bit selects input or output mode. In input mode, data on the SP pin is shifted into the shift register on the rising edge of the signal applied to the CNT pin. After 8 CNT pulses, the data in the shift register is dumped into the Serial Data Register and an interrupt is generated. In the output mode, TIMER A is used for the baud rate generator. Data is shifted out on the SP pin at 1/2 the underflow rate of TIMER A. The maximum baud rate possible is 02 divided by 6, but the maximum useable baud rate will be determined by line loading and the speed at which the receiver responds to input data. Transmission will start following a write to the Serial Data Register (provided TIMER A is running and in continuous mode). The clock signal derived from TIMER A appears as an output on the CNT pin. The data in the Serial Data Register will be loaded into the shfit register then shift out to the SP pin when a CNT pulse occurs. Data shifted out becomes valid on the falling edge of CNT and remains valid until the next falling edge. After 8 CNT pulses, an interrupt is generated to indicate more data can be sent. If the Serial Data Register was loaded with new information prior to this interrupt, the new data will automatically be loaded into the shift register and transmission will be continuous. If no further data is to be transmitted, after the 8th CNT pulse, CNT will return high and SP will remain at the level of the last data bit transmitted. SDR data is shifted out MSB first and serial input data should also appear in this format.

The bidirectional capability of the Serial Port and CNT clock allows several devices to be connected to a common serial communication bus on which one acts as a master, sourcing data and shift clock, while all other chips act as slaves. Both CNT and SP outputs are open drain, with passive pull-ups, to allow such a common bus. Protocol for slave/master selection can be transmitted over the serial bus, or via dedicated handshaking lines.

REG	Name								
C	SDR	S7	S6	S5	S4	S3	S2	S1	S0

Interrupt Control (ICR)

There are five sources of interrupts on the 8520: underflow from TIMER A, underflow from TIMER B, TOD ALARM, Serial Port full/empty and FLAG. A single register provides masking and interrupt information. The Interrupt Control Register consists of a write-only MASK register and a read-only DATA register. Any interrupt which is enabled by the MASK register will set the IR bit (MSB) of the DATA register and bring the IRQ pin low. In a multi-chip system, the IR bit can be polled to detect which chip has generated an interrupt request.

The interrupt DATA register is cleared and the IRQ line returns high following a read of the DATA register. Since each interrupt sets an interrupt bit regardless of the MASK, and each interrupt bit can be selectively masked to prevent the generation of a processor interrupt, it is possible to intermix polled interrupts with true interrupts. However, polling the IR bit will cause the DATA register to clear, therefore, it is up to the user to preserve the information contained in the DATA register if any polled interrupts were present.

The MASK register provides convenient control of individual mask bits. When writing to the MASK register, if bit 7 (SET/CLEAR) of the data written is a ZERO, any mask bit written with a one will be cleared, while those mask bits written with a zero will be unaffected. If bit 7 of the data written is a ONE, any mask bit written with a one will be set, while those mask bits written with a zero will be unaffected. In order for an interrupt flag to set IR and generate an Interrupt Request, corresponding MASK bit must be set.

READ (INT DATA)

REG	Name								
D	IRC	IR	0	0	FLG	SP	ALRM	TB	TA

WRITE (INT MASK)

REG	Name								
D	IRC	S/C	X	X	FLG	SP	ALRM	TB	TA

Control Registers

There are two control registers in the 8520: CRA and CRB. CRA is associated with TIMER A and CRB is associated with TIMER B.

CRA:

BIT	NAME	FUNCTION
0	START	1 = START TIMER A, 0 = STOP TIMER A. This bit is automatically reset when underflow occurs during one-shot mode.
1	PBON	1 = TIMER A output appears on PB6, 0 = PB6 normal operation.
2	OUTMODE	1 = TOGGLE, 0 = PULSE
3	RUNMODE	1 = ONE-SHOT, 0 = CONTINUOUS
4	LOAD	1 = FORCE LOAD (this is a STROBE input, there is no data storage, bit 4 will always read back a zero and writing a zero has no effect.
5	INMODE	1 = TIMER A counts positive CNT transitions, 0 = TIMER A counts 02 pulses.
6	SPMODE	1 = SERIAL PORT output (CNT sources shift clock). 0 = SERIAL PORT input (external shift clock required).
7	TODIN	1 = 50 Hz clock required on TOD pin for accurate time. 0 = 60 Hz clock required on TOD pin for accurate time.

CRB:

BIT	NAME	FUNCTION
		(Bits CRB0-CRB4 are identical to CRA0-CRA4 for TIMER B with the exception that bit 1 controls the output of TIMER B on PB7).
5.6	INMODE	Bits CRB5 and CRB6 select one of four input modes for TIMER B as:

CRB6	CRB5	
0	0	TIMER B counts 02 pulses.
0	1	TIMER B counts positive CNT transitions.
1	0	TIMER B counts TIMER A underflow pulses.
1	1	TIMER B counts TIMER A underflow pulses while CNT is high.

7	ALARM	1 = writing to TOD registers set ALARM, 0 = writing to TOD registers sets TOD clock.

ELECTRICAL PARAMETERS

Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the circuit. Functional operation of the device at these or any conditions other than those indicated in the operating conditions of the specification is not implied. Exposure to the maximum ratings for extended periods may adversely affect device reliability.

Supply Voltage	Vcc	−0.3V to 7.0V	Operating Temp.	Top	0°C to 70°C
Input/Output Voltage	Vin	−0.3V to 7.0V	Storage Temp.	Tstg	−55°C to 150°C

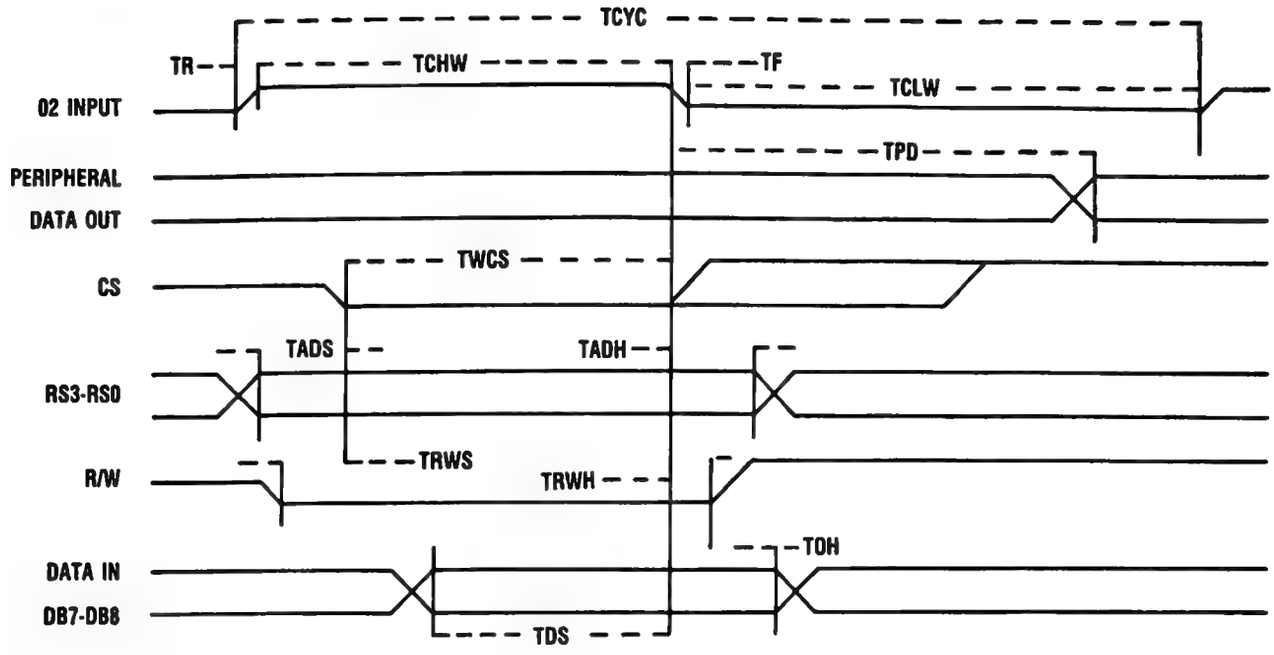
*All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

ELECTRICAL CHARACTERISTICS (VCC +/− 5%, VSS = 0v, TA = 0.70 C)

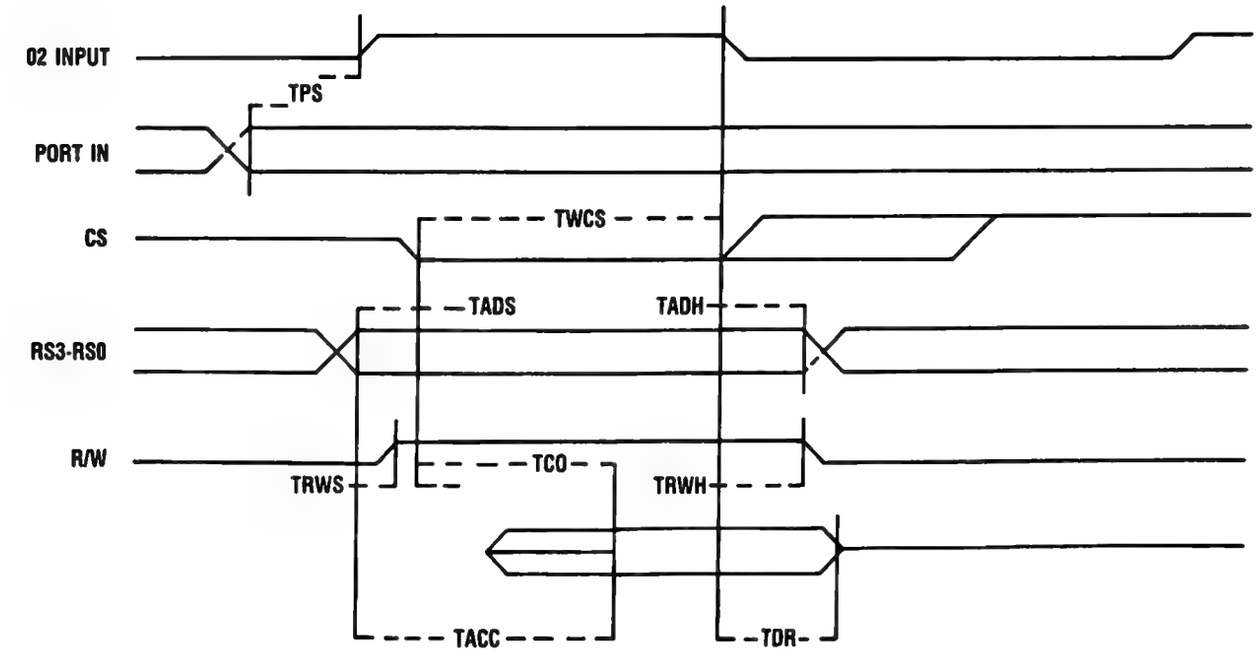
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage	Vih	+2.4	—	Vcc	V
Input Low Voltage	Vil	−3.0	—	+0.8	V
Input leakage current VIN = VSS + 5V (TOD, R/W, 02, RES, RS0-RS3, CS)	Iin	—	1.0	2.5	μA
PA0-7, PB0-7, TOD, FLAG, SP, CNT	Rpi	3.1	5.0	—	KΩ
Output leakage current for High Impedance State VIN = 4V to 2.4V (DB0-DB7, IRQ)	Itsi	—	±1.0	±10.0	μA
Output High Voltage VCC = MIN, LOAD < −200μA (PA0-PA7, DB0-DB7)	Voh	+2.4	—	Vcc	V
Output Low Voltage (PA0-PA7, DB0-DB7) VCC = MIN, LOAD<3.2μA	Vol	—	—	+0.40	V
Output High Current (sourcing) VOH>2.4V (PA0-PA7, DB0-DB7)	Ioh	−200	−1000	—	μA
Output Low Current (sinking) VOL<.4V (PA0-PA7, DB0-DB7)	Iol	3.2	—	—	μA
Output Low Current (sinking) VOL<.4V (PC, PB0-PB7)	Iol	13.0	—	—	μA
Input Capacitance	Cin	—	7	10	pf
Output Capacitance	Cout	—	7	10	pf
Power Supply Current	Icc	—	70	100	μA

TIMING DIAGRAMS

WRITE TIMING DIAGRAM



READ TIMING DIAGRAM



2.2 Timing Characteristics

SYMBOL	CHARACTERISTIC	1MHZ MIN	1MHZ MAX
	02 CLOCK		
TCYC	Cycle Time	1000	10,000
TR, TF	Rise and Fall Time	—	25
TCHW	Clock Pulse Width (High)	440	5,000
TCLW	Clock Pulse Width (Low)	440	5,000
	WRITE CYCLE		
TPD	Output Delay From 02	—	960
TWCS	CS low while 02 high	280	—
TADS	Address setup time	58	—
TADH	Address hold time	10	—
TRWS	R/W setup time	58	—
TRWH	R/W hold time	10	—
TDS	Data bus setup time	200	—
TDH	Data bus hold time	15	—
	READ CYCLE		
TPS	Port setup time	300	—
TWCS(2)	CS low while 02 high	280	—
TADS	Address setup time	58	—
TADH	Address hold time	10	—
TRWS	R/W setup time	58	—
TRWH	R/W hold time	10	—
TACC	Data access from RS3-RS0	—	300
TCO(3)	Data access from CS	—	240
TDR	Data release time	50	—

*See diagram on page 23 for timing relationships.

*NOTES:

1. All timings are referenced from VIL max and VIH min on inputs and VOL max and VOH min on outputs.
2. TWCS is measured from the later of 02 high or CS low. CS must be low at least until the end of 02 high.
3. TCO is measured from the later of 02 high or CS low. Valid data is available only after the later of TACC of TCO.

SECTION 3

TROUBLESHOOTING

A500/A2000 SYSTEM TEST

System Test is an auto-boot diskette. Once booted its own cli window will open. Type the commands listed below in order to run each test.

KEYTEST

- Full keyboard test
- press all keys to confirm proper operation
- click left mouse button in upper left corner to EXIT

KB

- Keyboard matrix test
- pressing the keys indicated by the program will test the matrix and seven dedicated key functions

SCREENTEST

- Screentest is low resolution graphic screen made up of 6 bit planes. Used to test RGB linearity and HALF BRIGHTS.
- screentest will display a RGB COLOR BAR scale and a 16 level gray scale in both normal and half bright mode. Normal scales are on top.
- Press space bar to EXIT screen.

SHOW.HIRES.TEST

- Hires.Test is a 4 bit plane high resolution 640 by 400 screen that displays NTSC color bars, 8 level gray scales, horizontal resolution lines, and an interlace test.
- Press space bar to EXIT screen.

SHOW BALLOON

- Balloon is a 6 bit plane hold and modify picture used to verify proper HAM decoding.
- This will test for a bad Agnus or Denise chip.
- Press space bar to EXIT screen.

CUBEROTE

- Cuberote is an animated cube whose speed and direction is controlled by the mouse X-Y position.The cube is blue with shading of three visible sides. Cuberote uses double buffering for a smooth animation. Direct manipulation of the Copper List permits the display of 16 shades blue while only using 2 bit planes.
- Click left mouse button in upper left corner to EXIT screen.

SYSTEST

- Systest will run the following test Realtime clock, Blit, Chip/Fast Ram Sprites/Bliter, and Disk I/O.
- Reboot computer to EXIT program.

Type the following for customizing systest.

SYSTEST 246d	; A500 NO A501	PCB
SYSTEST 2436cd	; A500 WITH A501 OR A2000	PCB
SYSTEST 1245679d	; A500 NO A501	BURN-IN
SYSTEST 12345679cd	; A500 WITH A501 OR A2000	BURN-IN
SYSTEST 12345678d	; A500 NO A501	AGING
SYSTEST 12345678cd	; A500 WITH A501 OR A2000	AGING

A500/A2000 SYSTEM TEST (Continued)

The system test may also be customized. Type the word SYSTEST then select any of the numeric alpha characters listed below.

1 _LOOP	Enable endless loop. This will test the real time clock and the blit only once. Then cycle through any of the selected test.
2 _BLIT	This will run BOXER as a background task for loading.
3 _EXTERNAL (FAST) RAM	This will test ram at $C00,000 and $200,000 to $9FF,FFF if found. If Fast ram is not detected program will pass but say FAST RAM NOT FOUND.
4 _EXTERNAL (CHIP) RAM	This is the same as FAST RAM test except that it test from $0 to $800,000.
5 _EXTENDED RAM TEST	This is an expanded version of Fast Ram. Along with unique address and refresh various bit patterns are used. These are All Zeros, All Ones, All A's and All 5's.
6 _DISK	In order to test the disk I/O. Tracks 2 and 8 will first be formatted. Upon successes $6DB6 will be written and verified from tracks 2 and 8.
7 _EXTENDED DISK	For Extended Disk all ONES, ALL ZEROS, $AAAA and $5555 are used.
8 _EXTRA DISK SEEK	During PCB and Burn-in testing this will seek only at a minimum. However during Aging test it will use maximum seeking.
9 _DISK CYCLE	This will test disk every 8 cycles if Loop test is also selected.
a _NO AUDIO	Disable Audio test.
b _NO SPRITES	Disable Sprite test.
c _CLOCK CHIP	This will test the real time clock chip.
d _DISPLAY GRAPHICS CLOCK	Displaying the graphics clock will test bliter indicating a bad agnus chip if display is corrupt.
f _BLITER LINE DRAW	This will test for extraneous bit set. Previously visual inspection of the graphics clock was used to test bliter. However now the line draw feature of agnus is tested through the program.

AMIGA 1.3 STARTUP SEQUENCE — OVERVIEW

1 - DELAY 1/3 SECOND (LET HARDWARE SETTLE)
2 - JUMP TO ROM CODE IN DIAG CART (IF FOUND)
3 - DISABLE/CLEAR ALL INTERRUPTS & DMA'S
4 - TURN ON SCREEN
5 - DISPLAY DARK GREY SCREEN — HARDWARE OK
6 - CHECKSUM ROM — IF BAD DISPLAY RED SCREEN
7 - SET UP TEMPORARY EXCEPTION PROCESSING — IF SPURIOUS EXCEPTION OCCUR, DISPLAY YELLOW SCREEN
8 - CONFIGURE LOCAL MEMORY (CHECK BOUNDARIES, SIZE) IF PROBLEM, DISPLAY GREEN SCREEN
9 - CHECK SOME CUSTOM IC REGISTERS — IF FAILURE, DISPLAY BLUE SCREEN
10 - RESTORE SCREEN — CHANGE TO LIGHT GREY = SOFTWARE OK

A500 SYSTEM TROUBLESHOOTING

SECTION 1 — BASIC PRELIMINARY CHECKS

There are a few basic checks which must be made on the A500 when troubleshooting a SYSTEM THAT DISPLAYS NO VIDEO ON POWER UP IN ANY AVAILABLE VIDEO MODE. There are several things which may cause this symptom but these BASIC SIGNALS MUST BE PRESENT in order for the system to operate. If all these Basic Checks seem correct, more Advanced Checks are covered in SECTIONS 2 THRU 3.

All signals must be taken with power applied to the system unless specified.

A (P) preceding the step number indicates signals which must be measured as power is applied to the system.

ALL MEASUREMENTS ARE WITHIN A ±10% TOLERANCE
ALL READINGS MUST BE TAKEN WITH AN OSCILLOSCOPE
(P) INDICATES SIGNALS WHICH MUST BE MEASURED ON SYSTEM POWER UP

STEP 1 Measure the voltage on pin 1 (right pin) on connector CN12
- Result = +5 VDC Level — Continue to Step 2

STEP 2 Measure the voltage on pin 4 (left pin) on connector CN12
- Result = +12 VDC Level — Continue to Step 3

STEP 3 Measure the voltage on pin 1 of IC U38 (MC1488)
- Result = −12 VDC Level — Continue to Step 4

If any result is incorrect, Refer to Section 1.1 TROUBLESHOOTING THE A500 SYSTEM POWER SUPPLY

(P) STEP 4 Measure the signal on pin 41 (RST)* of IC U5 (GARY)
- Result = 0 to +5 VDC shortly after system power up — Continue to Step 5

(P) STEP 5 Measure the signal on pin 11 (RESET)* of IC U37 (74LS32)
- Result = 0 to +5 VDC shortly after system power up — Continue to Step 6

(P) STEP 6 Measure the signal on pin 8 (IORESET)* of IC U37 (74LS32)
- Result = 0 to +5 VDC shortly after system power up — Continue to Step 7

If any result is incorrect, Refer to Section 1.2 TROUBLESHOOTING THE A500 SYSTEM RESET

STEP 7 Measure the signal on pin 15 (CLK) of IC U1 (68000)
- Result = 7 MHZ Clock — Continue to Step 8

STEP 8 Measure the signal on pin 4 (CCK)* of IC U33 (74F04)
- Result = Approximately 3.58 MHZ Clock — Continue to Step 9

STEP 9 Measure the signal on pin 6 (CCKQ)* of IC U33 (74F04)
- Result = Approximately 3.58 MHZ Clock — Continue to Step 10

STEP 10 Measure the signal on pin 10 (CDAC) of IC U33 (74F04)
- Result = Approximately 7 MHZ Clock — Continue to Section 2

If any result is incorrect, Refer to Section 1.3 TROUBLESHOOTING THE A500 SYSTEM CLOCKS

ALL THE SIGNALS LISTED, STEP 1 THROUGH STEP 10, MUST BE PRESENT FOR THE SYSTEM TO PRODUCE THE CORRECT VIDEO DISPLAY

IF ALL SIGNALS SEEM TO BE CORRECT, BEGIN THE STEPS LISTED IN SECTIONS 2 THROUGH 3 — TROUBLESHOOTING THE A500 CONTROL SIGNALS

*INDICATES ACTIVE LOW

A500 SYSTEM TROUBLESHOOTING (Continued)

SECTION 1.1 — TROUBLESHOOTING THE A500 SYSTEM POWER SUPPLY

By referring to this section, it is assumed that one or more of the +5 VDC, +12 VDC or −12 VDC measurements from BASIC PRELIMINARY CHECKS, STEPS 1 through 3 are incorrect.

LINE FILTER (LF1) PINOUTS — FROM FRONT OF PCB

Pin 4	Pin 3	Pin 2	Pin 1
★	★	★	★
+12V	+12V	−5V	GND
+12V	−12V	VCC	SH/GND
★	★	★	★
Pin 5	Pin 6	Pin 7	Pin 8

1.1.1 INCORRECT (+5) VDC SUPPLY

STEP 1 Disconnect the disk drive assembly and measure the voltage on pin 1 (right pin) of connector CN12

- Result = +5 VDC Level — Defective Drive Assembly
- Result = Incorrect — Continue to Step 2

STEP 2 Measure the voltage on pin 7 (VCC) of line filter (LF1)

- Result = +5 VDC Level — No +5 VDC Problem or Open +5 VDC Trace
- Result = Incorrect — Continue to Step 3

STEP 3 Measure the voltage on pin 2 (+5) of line filter (LF1)

- Result = +5 VDC Level — Defective Filter LF1
- Result = Incorrect — Defective Power Supply or Shorted Component

1.1.2 INCORRECT (+12) VDC SUPPLY

STEP 4 Disconnect the disk drive assembly and measure the voltage on pin 4 (left pin) of connector CN12

- Result = +12 VDC Level — Defective Drive Assembly
- Result = Incorrect — Continue to Step 5

STEP 5 Measure the voltage on pin 5 (+12V) of line filter (LF1)

- Result = +12 VDC Level — No +12 VDC Problem or Open +12 VDC Trace
- Result = Incorrect — Continue to Step 6

STEP 6 Measure the voltage on pin 4 (+12) of line filter (LF1)

- Result = +12 VDC Level — Defective Filter LF1
- Result = Incorrect — Defective Power Supply or Shorted Component

1.1.3 INCORRECT (−12) VDC SUPPLY

STEP 7 Measure the voltage on pin 6 (−12V) of line filter (LF1)

- Result = −12 VDC Level — No −12 VDC Problem or Open −12 VDC Trace
- Result = Incorrect — Continue to Step 8

STEP 8 Measure the voltage on pin 3 (−12V) of line filter (LF1)

- Result = −12 VDC Level — Defective Filter LF1
- Result = Incorrect — Defective Power Supply or Shorted Component

A500 SYSTEM TROUBLESHOOTING (Continued)

SECTION 1.2 — TROUBLESHOOTING THE A500 SYSTEM RESET

By referring to this section, it is assumed that one or more of the reset signals from BASIC PRELIMINARY CHECKS, STEPS 4 through 6 are incorrect.

1.2.1 INCORRECT (RST) RESET

(P) STEP 1	Measure the signal 5 (KBRESET)* of IC U5 (GARY)	
	• Result = 0 VDC to +5 VDC shortly after system power up	Continue to Step 2
	• Result = Incorrect	Continue to Step 1.1
(P) STEP 1.1	Measure the signal on collector of transistor Q711 (2N3904)	
	• Result = 0 VDC to +5 VDC Level shortly after power up	KBRESET OK or Open Reset Trace
	• Result = Incorrect	Continue to Step 1.2
(P) STEP 1.2	Measure the signal on pin 3 (OUT) of IC U42 (555)	
	• Result = +5 VDC to 0 VDC Level shortly after power up	Defective Q711, U5 Keyboard, Connector CN13
	• Result = Incorrect	Defective U42 or Associated Circuitry

1.2.2 INCORRECT (RESET) OR (IORESET) RESET

(P) STEP 2	Measure the signal on pin 12 (RST)* of IC U37 (74LS32)	
	• Result = 0 VDC to +5 VDC shortly after power up	Continue to Step 3
	• Result = Incorrect	Defective U5, U1, U2, U37
(P) STEP 3	Measure the signal on pin 11 (RESET)* of IC U37 (74LS32)	
	• Result = 0 VDC to +5 VDC shortly after system power up	RESET OK or Open Reset Trace
	• Result = Incorrect	Defective U37, U7, U8
(P) STEP 4	Measure the signal on pin 8 (IORESET)* of IC U37 (74LS32)	
	• Result = 0 VDC to +5 VDC Level shortly after power up	IORESET OK or Open Reset Trace
	• Result = Incorrect	Defective U37 Connector CN7

SECTION 1.3 — TROUBLESHOOTING THE A500 SYSTEM CLOCKS

1.3.1 INCORRECT (CLK) CLOCK

STEP 1	Measure the signal on pin 34 (28MHZ) of IC U2 (FAT AGNUS)	
	• Result = 28 MHZ Clock	Continue to Step 2
	• Result = Incorrect	Defective X1, U2
STEP 2	Measure the signal on pin 38 (7MHZ) of IC U2 (FAT AGNUS)	
	• Result = 7 MHZ Clock	CLK OK or Open Trace
	• Result = Incorrect	Defective U2, U1, U4

1.3.2 INCORRECT (CCK) CLOCK

STEP 3	Measure the signal on pin 28 (CCK) of IC U5 (GARY)	
	• Result = 3.58 MHZ Clock	Defective U33, U4
	• Result = Incorrect	Defective U5, U2, U3, U4, U33

1.3.3 INCORRECT (CCKQ) CLOCK

STEP 4	Measure the signal on pin 27 (CCKQ) of IC U5 (GARY)	
	• Result = 3.58 MHZ Clock	Defective U33
	• Result = Incorrect	Defective U5, U2, U3, U33

1.3.4 INCORRECT (CDAC) CLOCK

STEP 5	Measure the signal on pin 26 (CDAC)* of IC U5 (GARY)	
	• Result = 7 MHZ Clock	Defective U33
	• Result = Incorrect	Defective U5, U2, U4, U33

*INDICATES ACTIVE LOW

A500 SYSTEM TROUBLESHOOTING (Continued)

SECTION 2 — TROUBLESHOOTING THE MOTOROLA 68000 PROCESSOR

All initial power up signals must be processed by the 68000. In order for the correct power up sequence to take place, the 68000 control signals must be operating correctly.

Although the 68000 will probably initialize with signals of +2.5 VDC levels or above, a problem exists if control signals do not reach close to the +5 VDC levels.

STEP 1	Measure the signal on pin 17 (HLT)* of IC U1 (68000)	
	• Result = +5 VDC Level	Continue to Step 1.1
	• Result = Incorrect	Defective U1, U5
(P) STEP 2	Measure the signal on pin 18 (RST)* of IC U1 (68000)	
	• Result = 0 VDC to +5 VDC shortly after power up	Continue to Step 1.2
	• Result = Incorrect	See Section 1.2 Troubleshooting the A500 System Reset
(P) STEP 3	Measure the signal on pin 7-8 (UDS)*, (LDS)* of IC U1 (68000)	
	• Result = +5 VDC Level should start pulsing on initialization	Continue to Step 1.3
	• Result = Incorrect pin 7 (UDS)	Defective U1, U5, U2
	• Result = Incorrect pin 8 (LDS)	Defective U1, U5
(P) STEP 4	Measure the signal on pin 9 (R/_W)* of IC U1 (68000)	
	• Result = +5 VDC Level with Negative Pulsing	Continue to Step 1.4
	• Result = Incorrect	Defective U7, U8, U1, U5, U2
STEP 5	Measure the signal on pin 6 (AS)* of IC U1 (68000)	
	• Result = +5 VDC Sawtooth	Continue to Step 1.5
	• Result = Incorrect	Defective U1, U5, U2
STEP 6	Measure the signal on pin 10 (DTACK)* of IC U1 (68000)	
	• Result = +5 VDC Square Wave	Continue to Step 1.6
	• Result = Incorrect	Defective U1, U5
STEP 7	Measure the signal on pin 19,21 (VMA)* (VPA)* of IC U1 (68000)	
	• Result = +5 VDC Level with Negative Pulse	Continue to Step 1.7
	• Result = Incorrect pin 19 (VMA)	Defective U1
	• Result = Incorrect pin 21 (VPA)	Defective U1, U5
STEP 8	Measure the signal on pin 15 (CLK) of IC U1 (68000)	
	• Result = 7 MHZ Clock	Continue to Step 1.8
	• Result = Incorrect	See Section 1.3 Troubleshooting the A500 System Clock
STEP 9	Measure the signal on pin 20 (E) of IC U1 (68000)	
	• Result = +5 VDC Square Wave	Continue to Step 10
	• Result = Incorrect	Defective U7, U8, U1
(P) STEP 10	Measure the signal on pin 26,28 (FC2), (FC0) of IC U1 (68000)	
	• Result = +5 VDC to 0 VDC with positive pulses	Continue to Step 11
	• Result = Incorrect (Either or Both)	Defective U1, RP102
(P) STEP 11	Measure the signal on pin 27 (FC1) of IC U1 (68000)	
	• Result = +5 VDC on power up, then to 5 VDC pulsing	Continue to Step 12
	• Result = Incorrect	Defective U1, RP102
STEP 12	Measure the signal on pin 23 (IPL2)* of IC U1 (68000)	
	• Result = +5 VDC Level	Continue to Step 13
	• Result = Incorrect	Defective U1, U3, RP102

*INDICATES ACTIVE LOW

A500 SYSTEM TROUBLESHOOTING (Continued)

SECTION 2 — TROUBLESHOOTING THE MOTOROLA 68000 PROCESSOR (Continued)

STEP 13 Measure the signal on pin 24,25 (IPL1)*, (IPL0)* of IC U1 (68000)

• Result = +5 VDC with Negative Pulses	Continue to Step 14
• Result = Incorrect (Either or Both)	Defective U1, U3, RP102

STEP 14 Measure the signals on pins 22 (BEER)*, 12 (BGACK)*, 11 (BG)*, 13 (BA) of IC U1 (68000)

• Result = +5 VDC Level	Continue to Section 2.1
• Result = Incorrect pin 12 (BGACK)	Defective U1, U5, RP104
• Result = Incorrect pins 22, 11, 13	Defective U1, RP104

SECTION 3 — TROUBLESHOOTING THE A500 SYSTEM 8520 CIA's

STEP 1 Measure the signals on pins 23 (CS)*, 23 (CS)* of IC U7, U8 (8520)

• Result = +5 VDC Level with Negative Pusling	Continue to Step 2
• Result = Incorrect (U7 or U8)	Continue to Step 1.1

STEP 1.1 Measure the input to pin 5 (VMA)* of IC U37 (74LS32)

• Result = +5 VDC Level with Negative Pulsing	Continue to Step 1.2
• Result = Incorrect	Defective U1, U37, RP102

STEP 1.2 Measure the input to pin 4 (A13) of IC U37 (74LS32)

• Result = 5 V Pulsing Address	Defective U37, U7
• Result = Incorrect	U1, U2, U6

STEP 1.3 Measure the input to pin 1 (A12) of IC U37 (74LS32)

• Result = 5 V Pulsing Address	Defective U37, U8
• Result = Incorrect	U1, U2, U6

STEP 2 Measure the input to pin 22 (W)* of IC U8 (8520)

• Result = 5 V Pulsing - Should Stabilize on Work Bench Prompt display	Continue to Step 3
• Result = Incorrect	Defective U8, U7, U1, U5, U2

STEP 3 Measure the signal on pin 25 (E) of IC U7 and U8 (8520)

• Result = 5 V Pulsing	Continue to Step 4
• Result = Incorrect	Defective U7, U8, U1

STEP 4 Measure the signal on pin 21 (INT)* of IC U7 (8520)

• Result = +5 VDC Level - Negative Pulses during disk load	Continue to Step 5
• Result = Incorrect	Defective U8, U3

STEP 5 Measure the signal on pin 21 (INT)* of IC U8 (8520)

• Result = +5 VDC Level	Continue to Step 6
• Result = Incorrect	Defective U7, U3

STEP 6 Measure the signal on pin 19 (TICK)* of IC U7 (8520)

• Result = Standard Vertical Sync	Continue to Step 7
• Result = Incorrect	Defective U2, U7

STEP 7 Measure the signal on pin 19 (TICK)* of IC U8 (8520)

• Result = Standard Horizontal Sync	Continue to Step 8
• Result = Incorrect	Defective U2, U8

*INDICATES ACTIVE LOW

A500 SYSTEM TROUBLESHOOTING (Continued)

SECTION 4 — TROUBLESHOOTING THE A500 SYSTEM VIDEO

If all listed signals seem to be correct, the processor should be up and the system should be able to produce video information.

To make troubleshooting of the system video easier, both Analog RGB and Digital RGBI, as well as Composite Mode should be checked for proper operation.

> ***IMPORTANT: USE A KNOWN GOOD MONITOR AND CABLE***

SECTION 4.1 — INCORRECT OR NO DIGITAL VIDEO DISPLAYED

STEP 1 Measure the digital outputs (B0-B7) of IC U40, (B0-B3) of IC U41 (74HCT245)

- Result = Buffered RGBI Video — Defective RP402, CN9
- Result = Incorrect — Continue to Step 2

STEP 2 Measure the digital inputs (A0-A7) of IC U40, (A0-A3) of IC U41 (74HCT245)

- Result = Digital RGB Video — Defective U40, U41, HY1
- Result = Incorrect — Defective U4, U40, U41

SECTION 4.2 — INCORRECT OR NO ANALOG RGB VIDEO DISPLAYED

STEP 1 Measure the Analog Outputs (AR, AG, AB) of IC HY1 (VIDEO HYBRID)

- Result = Analog RGB Video — Defective EMI 431-433, CN9
- Result = Incorrect — Continue to Step 2

STEP 2 Measure the Digital Outputs (B0-B7) of IC U40, (B0-B3) of IC U41 (74HCT245)

- Result = Buffered RGBI Video — Defective HY1
- Result = Incorrect — Continue to Step 3

STEP 3 Measure the Digital Inputs (A0-A7) of IC U40, (A0-A3) of IC U41 (74HCT245)

- Result = Digital RGB Video — Defective U40, U41
- Result = Incorrect (U40) — Defective U4, U40, U41

SECTION 4.3 — INCORRECT OR NO COMPOSITE VIDEO DISPLAY

STEP 1 Measure the Composite Output (Comp) of IC HY1 (VIDEO HYBRID)

- Result = Composite Video and Sync — Defective EMI 435, CN10
- Result = Incorrect (Video) — Continue to Step 2
- Result = Incorrect (Sync) — Continue to Section 3.6

STEP 2 Measure the Digital Outputs (B0-B7) of IC U40, (B0-B3) of IC U41 (74HCT245)

- Result = Buffered RGBI Video — Defective HY1
- Result = Incorrect — Continue to Step 3

STEP 3 Measure the Digital Inputs (A0-A7) of IC U40, (A0-A3) of IC U41

- Result = Digital RGBI Video — Defective U40, U41
- Result = Incorrect — Defective U4, U40, U41

SECTION 4.4 — INCORRECT OR NO RGB VERTICAL SYNC

STEP 1 Measure the signal on pin 5 of RP403 (RESISTOR PACK)

- Result = Standard Vertical Sync — Defective RP403, CN9
- Result = Incorrect — Defective U2, RP403

SECTION 4.5 — INCORRECT OR NO RGB HORIZONTAL SYNC

STEP 1 Measure the signal on pin 3 of RP403 (RESISTOR PACK)

- Result = Standard Horizontal Sync — Defective RP403, CN9
- Result = Incorrect — Defective U2, RP403

A500 SYSTEM TROUBLESHOOTING (Continued)

SECTION 4.6 — INCORRECT OR NO COMPOSITE SYNC

STEP 1	Measure the signal on the output (B7) of IC U41 (74HCT245)	
	• Result = Standard Composite Sync	Defective HY1
	• Result = Incorrect	Continue to Step 2
STEP 2	Measure the signal on the input (A7) of IC U41 (74HCT245)	
	• Result = Standard Composite Sync	Defective U41
	• Result = Incorrect	Defective U2, U4, U41

SECTION 5 — TROUBLESHOOTING THE A500 SYSTEM INTERNAL DRIVE CIRCUITS

If video information is being displayed, but errors are encountered while trying to read from or write to the Internal Drive, the control signals to this circuitry should be checked for proper operation.

> ***IMPORTANT: USE A KNOWN GOOD DRIVE ASSEMBLY TO ELIMINATE THE DRIVE ITSELF AS THE POSSIBLE CAUSE OF ERRORS***

SECTION 5.1 — DRIVE MOTOR DOES NOT OPERATE CORRECTLY

STEP 1	Measure the signal on pin 7 (MTR)*, 16 (SEL)* of IC U5 (GARY)	
	• Result = High to Low Toggle = Motor On Stays High = Motor Off	Continue to Step 2
	• Result = Incorrect	Defective U8, U5
STEP 2	Measure the signal on pin 46 (MTRON) of IC U5 (GARY)	
	• Result = High = Motor On Low = Motor Off	Continue to Step 3
	• Result = Incorrect	Defective U5, U36
STEP 3	Measure the signal on pin 6 (MTR0)* of IC U36 (74LS38)	
	• Result = Low = Motor On High = Motor Off	Continue to Step 4
	• Result = Incorrect	Defective U36, Q503, CN11
STEP 4	Measure the signal on pin 12 (SIDE)* of IC U8 (8520)	
	• Result = High to Low Toggle = Motor On Stays High = Motor Off	Continue to Step 5
	• Result = Incorrect	Defective U8, CN11
STEP 5	Measure the signal on pin 10 (STEP)* of IC U8 (8520)	
	• Result = High Level with Negative Pulsing during motor on and head step time	Continue to Step 6
	• Result = Incorrect (U40)	Defective U8, CN11
STEP 6	Measure the signal on pin 24 (INDEX)* of IC U8 (8520)	
	• Result = High Level with Wide Negative Index Pulses	Continue to Step 7
	• Result = Incorrect	Defective U8, CN11
STEP 7	Measure the signal on pin 7 (RDY)* of IC U7 (8520)	
	• Result = High to Low Toggle = Motor On High Level = Motor Off	Continue to Step 8
	• Result = Incorrect	Defective U7, CN11
STEP 8	Measure the signal on pin 6 (TRK0)* of IC U7 (8520)	
	• Result = High to Low Toggle each time disk is inserted	Continue to Step 9
	• Result = Incorrect	Defective U7, CN11

* INDICATES ACTIVE LOW

A500 SYSTEM TROUBLESHOOTING (Continued)

SECTION 5.1 — TROUBLESHOOTING THE A500 SYSTEM INTERNAL DRIVE CIRCUITS (Continued)

STEP 9	Measure the signal on pin 5 (WPROT)* of IC U7 (8520)	
	• Result = Write-Protect OFF (Tab Closed - High Level) Write-Protect ON (Tab Open - High or Low Toggle) each time disk is inserted	Continue to Step 10
	• Result = Incorrect	Defective U7, CN11
STEP 10	Measure the signal on pin 4 (CHNG)* of IC U7 (8520)	
	• Result = High Level with Negative Pulsing each time disk is removed from drive	Continue to Step 11
	• Result = Incorrect	Defective U7, CN11
STEP 11	Measure the signal on pin 3 (LED)* of IC U7 (8520)	
	• Result = +5 VDC to 0 VDC Level when Power LED comes on	Replace Socketed ICs
	• Result = Incorrect	Defective U7, Q502, U33
STEP 12	Measure the signal on pin 37 (DKRD)* of IC U3 (PAULA)	
	• Result = +5 VDC Level with Negative Pulsing during disk read	Continue to Step 13
	• Result = Incorrect	Defective U3, CN11

ERROR DURING DISK WRITE

STEP 13	Measure the signal on pin 8 (DKWDB)* of IC U36 (74LS38)	
	• Result = +5 VDC Level with Negative Pulsing	Continue to Step 14
	• Result = Incorrect	Continue to Step 13.1
STEP 13.1	Measure the signal on pin 45 (DKWDB) of IC U5 (GARY)	
	• Result = 0 VDC Level with Positive Pulsing	Defective U36
	• Result = Incorrect	Continue to Step 13.2
STEP 13.2	Measure the signal on pin 38 (DKWD)* of IC U3 (PAULA)	
	• Result = +5 VDC Level with Negative Pulsing	Defective U5
	• Result = Incorrect	Defective U3, U5
STEP 14	Measure the signal on pin 11 (DKWEB)* of IC U36 (74LS38)	
	• Result = High to Low Toggle during disk write	Continue to Step 15
	• Result = Incorrect	Continue to Step 14.1
STEP 14.1	Measure the signal on pin 44 (DKWEB) of IC U5 (GARY)	
	• Result = Low to High Toggle during disk write	Defective U36, CN9
	• Result = Incorrect	Continue to Step 14.2
STEP 14.2	Measure the signal on pin 39 (DKWE) of IC U3 (PAULA)	
	• Result = Low to High Toggle during disk write	Defective U5
	• Result = Incorrect	Defective U3, U5

*INDICATES ACTIVE LOW

A500 SYSTEM TROUBLESHOOTING (Continued)

SECTION 6 — TROUBLESHOOTING THE A500 SYSTEM CONTROL PORTS

If the system reaches normal power up and errors are encountered while trying to access the icons or erratic mouse or joystick operation is encountered, the control port circuitry should be checked for proper operation.

Use a standard joystick for testing these ports.

> ***IMPORTANT: USE A KNOWN GOOD MOUSE OR JOYSTICK TO ELIMINATE THIS AS THE POSSIBLE CAUSE OF ERRORS***

CONTROL PORT 0 ERROR — CN1

STEP 1	Measure the input on pin 2 (1A) of IC U15 (72LS157)	
	• Result = +5 VDC to 0 VDC = UP	Continue to Step 2
	• Result = Incorrect	Defective U15, EMI411, RP401, CN1
STEP 2	Measure the input on pin 3 (1B) of IC U15 (74LS157)	
	• Result = +5 VDC to 0 VDC = LEFT	Continue to Step 3
	• Result = Incorrect	Defective U15, EMI412, RP401, CN1
STEP 3	Measure the input on pin 5 (2A) of IC U15 (74LS157)	
	• Result = +5 VDC to 0 VDC = DOWN	Continue to Step 4
	• Result = Incorrect	Defective U15, EMI413, RP401, CN1
STEP 4	Measure the input on pin 6 (2B) of IC U15 (74LS157)	
	• Result = +5 VDC to 0 VDC = RIGHT	Continue to Step 5
	• Result = Incorrect	Defective U15, EMI414, RP401, CN1
STEP 5	Measure the output on pin 2 (FIRE0) on EMI415	
	• Result = +5 VDC to 0 VDC = FIRE	Continue to Step 6
	• Result = Incorrect	Defective EMI415, U7, CN1
STEP 6	Measure the output on pin 4 (1Y) of IC U15 (74LS157)	
	• Result = +5 VDC Level = CENTER Multiplexed Output = UP/LEFT	Continue to Step 7
	• Result = Incorrect	Defective U15, U4, RP404, RP405
STEP 7	Measure the output on pin 7 (2Y) of IC U15 (74LS157)	
	• Result = +5 VDC Level = CENTER Multiplexed Output = RIGHT/DOWN	Control Port 0 OK
	• Result = Incorrect	Defective U15, U4, RP404, RP405

CONTROL PORT 1 ERROR — CN2

STEP 1	Measure the input on pin 11 (3A) of IC U15 (74LS157)	
	• Result = +5 VDC to 0 VDC = UP	Continue to Step 2
	• Result = Incorrect	Defective U15, EMI421, RP401, CN2
STEP 2	Measure the input on pin 10 (3B) of IC U15 (74LS157)	
	• Result = +5 VDC Level to 0 VDC = LEFT	Continue to Step 3
	• Result = Incorrect	Defective U15, EMI422, RP401, CN2
STEP 3	Measure the input on pin 14 (4A) of IC U15 (74LS157)	
	• Result = +5 VDC to 0 VDC = DOWN	Continue to Step 4
	• Result = Incorrect	Defective U15, EMI423, RP401, CN2
STEP 4	Measure the input on pin 13 (4B) of IC U15 (74LS157)	
	• Result = +5 VDC to 0 VDC = RIGHT	Continue to Step 5
	• Result = Incorrect	Defective U15, EMI424, RP401, CN2

A500 SYSTEM TROUBLESHOOTING (Continued)

SECTION 6 — TROUBLESHOOTING THE A500 SYSTEM CONTROL PORTS (Continued)

STEP 5	Measure the output on pin 2 (FIRE1) of EMI425	
	• Result = +5 VDC to 0 VDC = FIRE	Continue to Step 6
	• Result = Incorrect	Defective EMI425, U7, CN2
STEP 6	Measure the output on pin 9 (3Y) of IC U15 (74LS157)	
	• Result = +5 VDC Level = CENTER Multiplexed Output = UP/LEFT	Continue to Step 7
	• Result = Incorrect	Defective U15, U4, RP404, RP405
STEP 7	Measure the output on pin 12 (4Y) of IC U15 (74LS157)	
	• Result = +5 VDC Level = CENTER Multiplexed Output = RIGHT/DOWN	Control Port 1 OK
	• Result = Incorrect	Defective U15, U4, RP404, RP405

SECTION 7 — TROUBLESHOOTING THE A500 SYSTEM KEYBOARD CIRCUITS

If the LED located on the Shift/Lock key goes into a flash code on power up, a failure in the keyboard circuitry is normally indicated. The circuitry located on the physical keyboard is normally at fault when this condition is encountered.

FLASH CODE FAILURE CHART

1 FLASH	= ROM	(Internal to the Keyboard Processor)
2 FLASHES	= RAM	(Internal to the Keyboard Processor)
3 FLASHES	= WATCHDOG TIMER	(IC 74LS123 or Associated Circuitry)

If no flashes are displayed or the keyboard is not the cause of the problem, troubleshooting of the main PCB keyboard circuitry will be necessary.

KEYBOARD CONNECTOR (CN13) PINOUTS — FROM FRONT OF PCB

Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
★	★	★	★	★	★	★	★
KBDATA	CLOCK	RESET	+5V	KEY	GROUND	STATUS	INUSE

STEP 1	Measure the signal on pins 2 (KBDATA)*, 1 (KBCLOCK)* of Connector CN13	
	• Result = +5 VDC Level - Negative Pulsing when key is depressed	Continue to Step 2
	• Result = Incorrect	Defective U7, RP501, CN13
STEP 2	Measure the signal on pin 3 (KBRESET)* of Connector CN13	
	• Result = 0 VDC to +5 VDC shortly after system power up	Continue to Step 3
	• Result = Incorrect	Refer to Section 1.2 — A500 System Reset
STEP 3	Measure the signal on pin 7 (STATUS) of Connector CN13	
	• Result = 0 VDC to +5 VDC when Power LED comes on	Continue to Step 4
	• Result = Incorrect	Continue to Step 3.1
STEP 3.1	Measure the signal on pin 3 (LED)* of IC U7 (8520)	
	• Result = +5 VDC to 0 VDC when Power LED comes on	Defective Q502 or Associated Circuitry
	• Result = Incorrect	Defective U7, Q502, U38
STEP 4	Measure the signal on pin 8 (INUSE) of Connector CN13	
	• Result = 0 VDC Level - Toggles High each time disk inserted	Keyboard OK
	• Result = Incorrect	Continue to Step 4.1
STEP 4.1	Measure the signal on pin 6 (MTR0)* of IC U36 (74LS38)	
	• Result = Low = Motor On High = Motor Off	Defective Q503 or Associated Circuitry
	• Result = Incorrect	Defective U36, Q503

*INDICATES ACTIVE LOW

A500 SYSTEM TROUBLESHOOTING (Continued)

SECTION 8 — TROUBLESHOOTING THE A500 SYSTEM AUDIO CIRCUITS

In order to determine failures in the audio circuitry it is necessary to generate some type of audio output while checking signals. Selecting the Music Icon from the Extras Disk will work to accomplish this.

If both channels are failing it is recommended that a Dual Trace Scope be used for audio troubleshooting. If only one channel is failing, using a single trace of the scope should be sufficient.

INCORRECT LEFT AUDIO CHANNEL

STEP 1	Measure the signal on pin 31 (LEFT) of IC U3 (PAULA)	
	• Result = Approximately 100 mV Audio	Continue to Step 2
	• Result = Incorrect	Defective U3, U14, EMI306
STEP 2	Measure the input to pin 13 (−) of IC U14 (LF347)	
	• Result = Approximately 100 mV Audio	Continue to Step 3
	• Result = Incorrect	Defective EMI306, U14 or Associated Circuitry
STEP 3	Measure the output on pin 14 of IC U14	
	• Result = Approximately 1-2 V Audio	Continue to Step 4
	• Result = Incorrect	Defective U14 or Associated Circuitry
STEP 4	Measure the input to pin 3 (+) of IC U14	
	• Result = Approximately 1-2 V Audio	Continue to Step 5
	• Result = Incorrect	Defective R322, R323
STEP 5	Measure the output on pin 1 of IC U14	
	• Result = Approximately 1-2 V Audio	Continue to Step 6
	• Result = Incorrect	Defective U14 or Associated Circuitry
STEP 6	Measure the signal on pin 1 of EMI302	
	• Result = Approximately 100 mV Audio	Continue to Step 7
	• Result = Incorrect	Defective C324, C325, R324, R325, EMI302
STEP 7	Measure the signal on pin 2 (LEFT), of EMI302	
	• Result = Approximately 200 mV Audio	Defective CN4
	• Result = Incorrect	Defective EMI302, CN3

INCORRECT RIGHT AUDIO CHANNEL

STEP 1	Measure the signal on pin 30 (RIGHT) of IC U3 (PAULA)	
	• Result = Approximately 100 mV Audio	Continue to Step 2
	• Result = Incorrect	Defective U3, U14, EMI305
STEP 2	Measure the input to pin 9 (−) of IC U14 (LF347)	
	• Result = Approximately 100 mV Audio	Continue to Step 3
	• Result = Incorrect	Defective EMI305, U14 or Associated Circuitry
STEP 3	Measure the output on pin 8 of IC U14 (LF347)	
	• Result = Approximately 1-2 V Audio	Continue to Step 4
	• Result = Incorrect	Defective U14 or Associated Circuitry
STEP 4	Measure the input to pin 5 (+) of IC U14 (LF347)	
	• Result = Approximately 1-2 V Audio	Continue to Step 5
	• Result = Incorrect	Defective R332, R333
STEP 5	Measure the output on pin 7 of IC U14 (LF347)	
	• Result = Approximately 1-2 V Audio	Continue to Step 6
	• Result = Incorrect	Defective U14 or Associated Circuitry
STEP 6	Measure the signal on pin 1 of EMI303	
	• Result = Approximately 100 mV Audio	Continue to Step 7
	• Result = Incorrect	Defective C334, C335, R334, R335, EMI303
STEP 7	Measure the signal on pin 2 (RIGHT) of EMI303	
	• Result = Approximately 200 mV Audio	Audio OK or Defective CN3
	• Result = Incorrect	Defective EMI303, CN3

A500 SYSTEM TROUBLESHOOTING (Continued)

SECTION 9 — TROUBLESHOOTING THE A500 SYSTEM CENTRONICS PORT

When all control signal to the 8520 CIAs are confirmed good, (See Section 2), the Centronics Parallel Port should be operational. To verify proper operation of this port it is necessary to connect a printer and load software to access it. Signals should be measured as the printer is being accessed.

STEP 1	Measure the signals on pin 2 (D0-D7) of EMI512 through EMI519	
	• Result = +5 VDC Level on normal power up will become active when the printer is accessed	Continue to Step 2
	• Result = Incorrect	Continue to Step 1.1
STEP 1.1	Measure the signals on pin 1 (PB0-PB7) of EMI512 through EMI519	
	• Result = +5 VDC Level on normal power up will become active when the printer is accessed	Defective EMI512 - EMI519
	• Result = Incorrect	Defective U7, EMI512 - EMI519
STEP 2	Measure the signals on pins 2 (STROBE)*, (ACK)* of EMI511, EMI521	
	• Result = +5 VDC Level on normal power up will become active when the printer is accessed	Continue to Step 3
	• Result = Incorrect	Continue to Step 2.1
STEP 2.1	Measure the signals on pins 1 (PC)*, (F)* of EMI511, EMI521	
	• Result = +5 VDC Level on normal power up will become active when the printer is accessed	Defective EMI511, EMI521
	• Result = Incorrect	Defective U7, EMI511, EMI521
STEP 3	Measure the signals on pin 2 (BUSY), (POUT), (SEL) of EMI522 - EMI524	
	• Result = +5 VDC Level on normal power up will become active when the printer is accessed	Continue to Step 4
	• Result = Incorrect	Continue to Step 3.1
STEP 3.1	Measure the signals on pin 1 (PA0-PA2) of EMI522 - EMI524	
	• Result = +5 VDC Level on normal power up will become active when the printer is accessed	Defective EMI522 - EMI524
	• Result = Incorrect	Defective U8, EMI522 - EMI524
STEP 4	All outputs seem correct	Replace U7, U8 and check Connector CN7

SECTION 10 — TROUBLESHOOTING THE A500 SYSTEM RS232 PORT

When all control signal to the 8520 CIAs are confirmed good, (See Section 2), the RS232 Serial Port should be operational. To verify proper operation of this port it is necessary to connect a printer and load software to access it. Signals should be measured as the printer is being accessed.

STEP 1	Measure the signals on pins 2 (TxD), (RTS) of EMI532 through EMI533	
	• Result = +5 VDC Level on normal power up will become active when the printer is accessed	Continue to Step 2
	• Result = Incorrect	Continue to Step 1.1
STEP 1.1	Measure the signals on pins 4, 9 (PA6), (TxD)* of IC U38 (1488)	
	• Result = +5 VDC Level on normal power up will become active when the printer is accessed	Defective U38, EMI533,532
	• Result = Incorrect (PA6)	Defective U8, U38
	• Result = Incorrect (TxD)	Defective U3, U38

*INDICATES ACTIVE LOW

A500 SYSTEM TROUBLESHOOTING (Continued)

SECTION 10 — TROUBLESHOOTING THE A500 SYSTEM RS232 PORT (Continued)

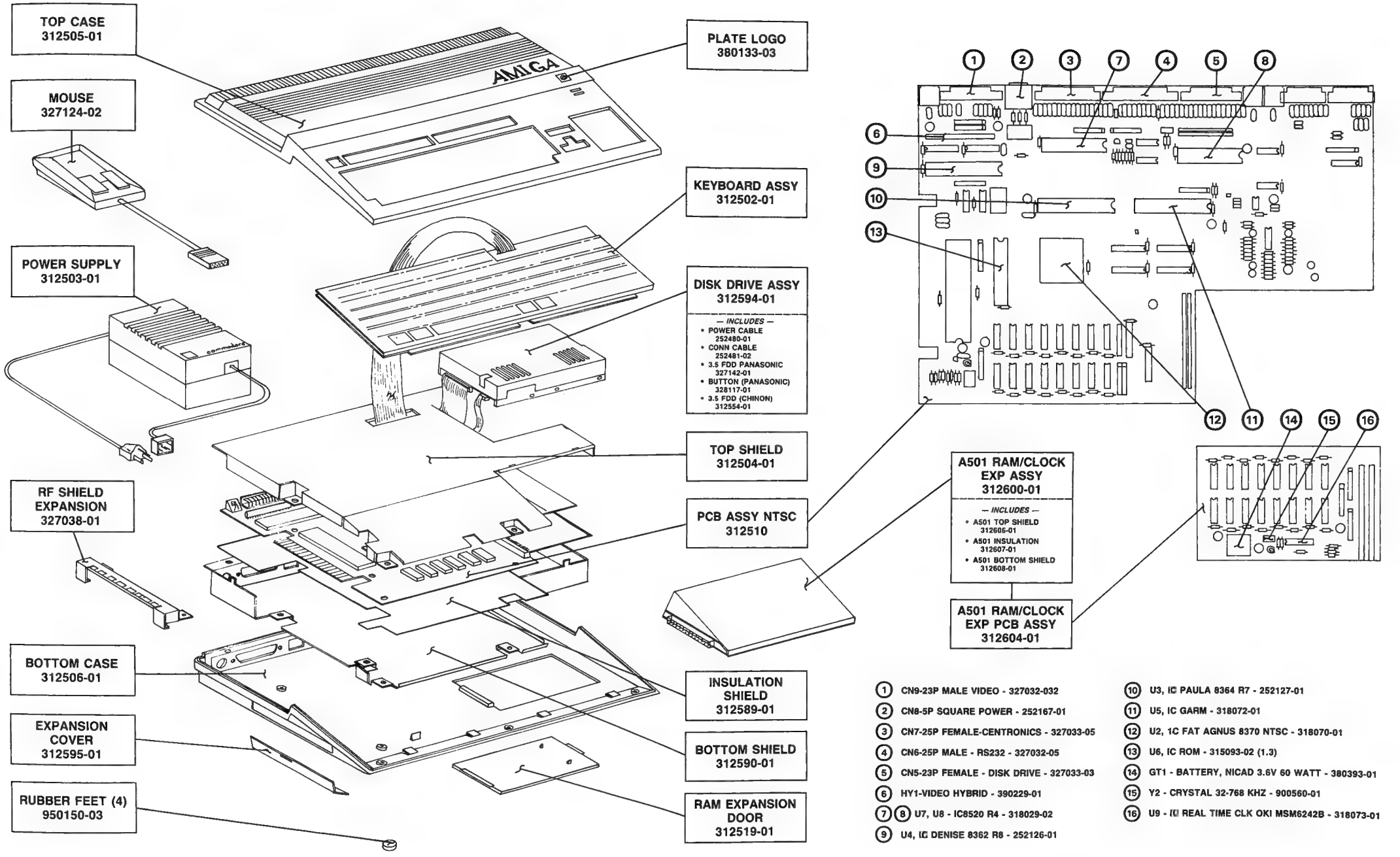
STEP 2	Measure the signal on pin 1 (DTR) of EMI531	
	• Result = +5 VDC Level on normal power up will become active when the printer is accessed	Continue to Step 3
	• Result = Incorrect	Continue to Step 2.1
STEP 2.1	Measure the signal on pin 12 (PA7) of IC U38 (1488)	
	• Result = +5 VDC Level on normal power up will become active when the printer is accessed	Defective U38, EMI531
	• Result = Incorrect	Defective U8, U38
STEP 3	Measure the signals on pins 5-7 (PA3-PA5) of IC U8 (8520)	
	• Result = +5 VDC Level on normal power up will become active when the printer is accessed	Continue to Step 4
	• Result = Incorrect	Defective U39, U8, EMI535 - EMI537
STEP 4	Measure the signal on pins 3 (RxD)* of IC U39 (1489)	
	• Result = +5 VDC Level on normal power up will become active when the printer is accessed	Continue to Step 5
	• Result = Incorrect	Defective 39, U3
STEP 5	All signals seem correct	Replace U8, U3, U38, U39

*INDICATES ACTIVE LOW

SECTION 4

PARTS

SERVICE PARTS REFERENCE DIAGRAM



A500 MAJOR COMPONENT PARTS LIST

Power Cable FDD	C	252480-01
Conn Cable FDD	C	252481-02
Keyboard Assy — USA/Canada	C	312502-01
Power Supply	C	312503-01
Top Shield	C	312504-01
Top Case	C	312505-01
Bottom Case	C	312506-01
PCB Assy — NTSC	C	312510-01
RAM Expansion Door	C	312519-01
Floppy Disk Drive (Chinon)	C	312554-01
Insulation Sheet	C	312589-01
Bottom Shield	C	312590-01
Disk Drive Assy	C	312594-01
Expansion Cover	C	312595-01
A501 RAM/Clock PCB Assy (With Shields)	C	312600-01
A501 RAM/CLK PCB Assy (PCB Only)	C	312604-01
A501 Top Shield		312606-01
A501 Insulation Sheet		312607-01
A501 Bottom Shield		312608-01
Service Manual	C	314981-01
Users Guide, DOS Manual	C	317100-01
Amiga Basic Diskette	C	317488-02
Workbench Diskette	C	317608-01
RF Shield Expansion	C	327038-01
Amiga Basic Manual	C	327102-01
Mouse	C	327124-02
Floppy Disk Drive (Panasonic)	C	327142-01
Button (Panasonic)	C	328117-01
Plate Logo	C	380133-03
Rubber Feet	C	950150-03

C - Indicates Commodore Stocked Part Number

COMPONENT PARTS LIST
PCB ASSEMBLY #321510, A500, REV. 5

321510-05 PCB ASSY, A500 NTSC 321510-06 PCB ASSY, A500 PAL

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IC COMPONENTS		
390084-03	M68000, 8 MHz	U1
318070-01	FAT AGNUS, 8370R3 NTSC	U2
318071-01	FAT AGNUS, 8371R1, PAL	U2
252127-02	PAULA, 8364R7	U3
252126-02	DENISE, 8362R8	U4
318072-01	GARY 5719	U5
318029-01	8520R4	U5
315093-01	ROM, KICKSTART V1.3	U5
390226-01	256K X 1 BIT DYNAMIC RAM	U16-U31
380223-01	256K X 1 BIT DYNAMIC RAM	U16-U31
901882-01	1488	U38
901883-01	1489	U39
390086-01	LF347/TL084	U14
390110-01	74F04	U33
901521-31	74LS32	U37
901521-38	74LS38	U36
390081-01	74F74	U32
901521-11	74LS157	U15
318050-01	74F244	U34,U35
901521-13	74LS244	U10,U12
310003-01	74HC245	U40,U41
901521-29	74LK373	U11,U13
901523-01	NE555	U42
252126-01	DENISE, 8362R6	U4
380223-05	DRAM, 256K X 1 BIT, 80ns	U16-U31

CONNECTORS		
252167-01	DIN, 5 PIN, SQUARE, FEMALE	CNB
390242-01	D-SUB, 9 PIN, MALE, RA, SOLDER-IN	CN1,CN2
390242-03	D-SUB, 23 PIN, MALE, RA, SOLDER-IN	CN9
390241-03	D-SUB/23PIN/FEMALE/RA/SOLDER-IN	CN5
390242-05	D-SUB/25PIN/MALE/RA/SOLDER-IN	CN6
390241-05	D-SUB/25PIN/FEMALE/RA/SOLDER-IN	CN7
252122-04	RCA JACK, BLACK	CN3
252122-01	RCA JACK, WHITE	CN4
252122-03	RCA JACK, YELLOW	CN10
390248-01	RCA JACK, METAL	CN3,CN4,CN10
325516-04	HEADER, 4PIN, POLARIZED, SIL	CN12
903326-08	HEADER, 8PIN, SIL	CN13
903345-17	HEADER, 34PIN, DIL	CN11
390224-01	HEADER/DUAL/RA/LONG/56POS/MALE	CNX

RESISTORS		
902410-18	NETWORK, 10K X 9 10PIN	RP501
390227-03	NETWORK, 22 OHM X 5, 10PIN	RP103
902422-05	NETWORK, 47 OHM X 4, 8PIN	RP102,RP403
902422-06	NETWORK, 68 OHM X 4, 8PIN	RP210,RP202
390227-05	NETWORK, 68 OHM X 5, 10PIN	RP203
902441-10	NETWORK, 120 OHM X 5, 6PIN	RP405
902442-17	NETWORK, 470 OHM X 7, 8PIN	RP104
902410-08	NETWORK, 4.7K X 9, 10PIN	RP101,RP102,RP401, RP501
902422-06	NETWORK, 68 OHM X 4, 8PIN	RP404
390186-01	ZERO OHM RESISTOR	W1,W2
901550-118	1 OHM, 5% 1/4W	EM1301,EM1406
901550-129	5.1 OHM, 5% 1/4W	EM1401,R405,R406
901550-64	10 OHM, 5% 1/4W	R301,R302
901550-90	27 OHM, 5% 1/4W	R101,R102
901600-15	47 OHM, 5% 1/2W	EM1501,EM1503
901550-108	360 OHM, 5% 1/4W	R331,4321
901550-57	390 OHM, 5% 1/4W	R325,R335
901550-58	470 OHM, 5% 1/4W	R305
901550-01	1K OHM, 5% 1/4W	R303,R304,R324,R334, R713,R305
901550-17	1.2K OHM, 5% 1/4W	R704
901550-23	2.7K OHM, 5% 1/4W	R701
901550-39	3.9K OHM, 5% 1/4W	R702
901550-19	4.7K OHM, 5% 1/4W	R402,R403,R502-R504
901550-20	10K OHM, 5% 1/4W	R322,R323,R333,R339, R501,R505,R506
901550-15	27K OHM, 5% 1/4W	R703

RESISTORS *(Continued)*		
901550-22	47K OHM, 5% 1/4W	R712
901550-84	1M OHM, 5% 1/4W	R711
901550-75	120 OHM, 5% 1/4W	R103-R108
901550-20	10K OHM, 5% 1/4W	R306,R308
901550-23	2.7K OHM, 5% 1/4W	R307
901550-82	470K OHM, 5% 1/4W	R326,R336
901550-89	150 OHM, 5% 1/4W	R409

BEADS/FILTERS		
252133-01	FERRITE BEAD	RB801,RB802
903025-01	FERRITE BEAD	FB802,FB801, EMI411-EMI417, EMI421-EMI427
903025-01	FERRITE BEAD	FB802,FB101 EMI411-EMI417, EMI421-EMI427, EMI402-EMI431-EMI435
251842-02	EMI FILTER, 100 pf	EMI301-EMI303, EMI401-EMI405, EMI411-EMI417, EMI421-EMI427, EMI431-EMI435, EMI511-EMI538, EMI601-EMI611-EMI626,EMI701-EMI704
251842-02	EMI FILTER, 100 pf	EMI101,EMI302, EMI303,EMI305, EMI306,EMI402-EMI404,EMI407, EMI431-EMI435, EMI511-EMI524, EMI531-EMI538, EMI601,EMI611-EMI626,EMI702-EMI704
251842-02	EMI FILTER, 100 pf	EMI101,EMI302, EMI303,EMI305, EMI306,EMI403-EMI407,EMI511-EMI524,EMI531-EMI538,EMI601, EMI602,EMI611-EMI626,EMI701, EMI702

CAPACITORS		
900462-27	39 pF, MLC, AXIAL, NPO	C703
900462-37	100 pF, MLC, AXIAL, NOP	C704
900463-16	1000 pF MLC AXIAL X7R	C705
900463-16	1000 pF MLC AXIAL X7R	C411-C413,C421-C423
900463-23	3900 pF MLC AXIAL X7R	C323,C333
900463-26	6800 pF MLC AXIAL X7R	C322,C332
390082-02	.01 uF MLC AXIAL Z5U	C410,C412,C801,C713
390082-02	.01 uF MLC AXIAL Z5U	C308,C713
900463-36	.047 uF MLC AXIAL X7R	C311-C314
390082-01	.1 uF MLC AXIAL Z5U	C7,C8,C10,C11-C13, C15,C33-C37,C39, C321,C331,C711, C701(-01 & -02)
390082-05	.22 uF MLC AXIAL Z5U	C1-C6,C16-C32,C14, C40-C42,C301,C302, C305,C501,C502
390082-05	.22 uF MLC AXIAL Z5U	C325,C335
390101-06	10 uF ELECT RADIAL	C306,C712
390101-04	22 uF ELECT RADIAL	C303,C304,C307,C334
390101-01	47 uF ELECT RADIAL	C812-C815,C821,C822
390101-02	100 uF ELECT RADIAL	C307,C811
900100-56	3300 uF 10 V ELECT RADIAL	C401,C402
251029-06	VARIABLE CAP 4.5-45 pf	C702

COMPONENT PARTS LIST
PCB ASSEMBLY #321510, A500, REV. 5 *(Continued)*

TRANSISTORS/DIODES		
390239-01	TRANS 2N5770 NPN OSC.	Q701
902658-01	TRANS 2N3904 NPN GP	Q501,Q711
902707-01	TRANS 2N3906 PNP GP	Q502,Q503,Q301
390254-01	TRANS JFET PN4302 MPF-102	Q321,Q331
900850-01	DIODE, 1N4148	D501
CRYSTALS		
900556-11	28.63636 MHz	Y1
900556-12	28.37516 MHz	Y1
325566-14	OSCILLATOR, 28.63636 MHz	X1
252344-01	OSCILLATOR, 28.37515 MHz	X1
MISCELLANEOUS		
390229-02	VIDEO HYBRID	HY1
390229-01	VIDEO HYBRID	HY1
251878-02	LINE FILTER, 8PIN	LF1
901151-19	CHOKE, 3.3 uH	L701

MISCELLANEOUS *(Continued)*		
904150-06	SOCKET, 40 PIN DIP	U6-U8
251313-01	SOCKET, 48 PIN DIP	U3-U5
251313-02	SOCKET, 48 PIN DIP	U3-U5
390185-01	SOCKET, 84 PIN PLCC	U2
904150-10	SOCKET, 64 PIN DIP	U1
312519-01	WIRE ASSEMBLY JUMPER	
900462-37	CAP 100 pF MLC AXIAL NOP	C101,R106,R107,R108, R103,EMI402
390082-02	CAP 0.01 uF MLC AXIAL Z5U	C801-C803
380223-03	IC, 256K X 1 BIT DYNAMIC RAM	U16-U31
390226-03	IC, 256K X 1 BIT DYNAMIC RAM	U16-U31
390226-05	IC, 256K X 1 BIT DYNAMIC RAM	U16-U31
901550-94	RES 68 OHM 5% 1/4W	
900463-36	CAP .047 uF MLC AXIAL X7R	
320481-01	SHRINK TUBING .50 IN. LG.	
312511-01	SCHEMATIC	

COMPONENT PARTS LIST
PCB ASSEMBLY #312510, AMIGA A500, REV6A/7

312510-07 PCB ASSEMBLY, A500 NTSC **312510-08 PCB ASSEMBLY, A500 PAL**

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IC COMPONENTS		
901882-01	INTERFACE MC1488	U38
901883-03	INTERFACE MC1489	U39
390086-01	LINEAR LF347/TL084	U14
901523-01	LINEAR NE555	U42
390084-03	MC68000 OMHz	U1
318072-01	MOS 5719 R2 GARY	U5
252126-02	MOS 8362 R8 DENISE	U4
252127-02	MOS 8364 R7 PAULA	U3
318069-02	MOS 8372 R3 AGNUS HR	U2
318029-02	MOS 8520 R4 AMIGA CIA	U7,U8
390110-01	TTL 74F04	U33
318050-01	TTL 74F244	U34,U35
310003-01	TTL 74HC245	U40,U41
901521-11	TTL 74LS157	U15
901521-13	TTL 74LS244	U10,U12
901521-31	TTL 74LS32	U37
901521-29	TTL 74LS373	U11,U13
901521-38	TTL 74LS38	U36
390229-01	VIDEO HYBRID	HY1
318070-01	MOS 8370 R3 FAT AGNUS (NTSC)	U2
318071-01	MOS 8371 R1 FAT AGNUS (PAL)	U2
390433-01	MOS 8373 R2 DENISE HR	U4
381099-04	DRAM 256K X 4 120 nS	U16-U19
381099-02	DRAM 256K X 4 100 nS	U16-U19
	NOT LOADED	U20-U23
395093-02	ROM 256K X 16 KICKSTART 1.3	U6

CAPACITORS		
900462-29	MLC AXIAL NOP 47pF	C403
900462-29	MLC AXIAL NOP 47pF	E102,E103,E106-3109
900462-29	MLC AXIAL NOP 47pF	XC1-XC3
900463-16	MLC AXIAL X7R 1000pF	C411-C413,C421-C423
900463-23	MLC AXIAL X7R 3900pF	C323,C333
900463-26	MLC AXIAL X7R 6800pF	C322,C332
900463-36	MLC AXIAL X7R .047pF	C311-C314
900463-37	MLC AXIAL X7R .1uF	C321,C331
390082-01	MLC AXIAL Z5U .01uF	C308,C713,C800-C803
390082-02	MLC AXIAL Z5U .1uF	C711
390082-04	MLC AXIAL Z5U .33uF	C1-C8,C10-C19,C33-C37,C39-C42,C301,C302,C305,C325,C335,C501,C502,C701,C804
	NOT LOADED	C20-C23
390101-06	ELECT ALUM RADIAL, 10uF 16V	C306,C712
390101-04	ELECT ALUM RADIAL, 22uF 35V	C303,C304,C324,C334
390101-01	ELECT ALUM RADIAL, 47uF 35V	C821,C822
390101-02	ELECT ALUM RADIAL, 100uF 16V	C811-C816
390101-03	ELECT ALUM RADIAL 470uF 16V	C307
900100-56	ELECT ALUM RADIAL 3300uF 10V	C401,C402

CONNECTORS		
325516-04	4PIN FLOPPY POWER	CN12
252167-01	5PIN SQ DIN	CN8
903335-08	8PIN SIL W/KEY	CN13
390241-03	D-SUB/23PIN/FEMALE/DB23S	CN5
390242-03	D-SUB/23PIN/MALE/DB23P	CN9
290241-05	D-SUB/25PIN/FEMALE/DE25S	CN7
290242-05	D-SUB/25PIN/MALE/DB25P	CN6
390242-01	D-SUB/9PIN/MALE/DB9P	CN1,CN2
350903-01	HEADER 34PIN W/KEY	CN11
390224-07	HEADER 56PIN MALE RA	CNX
252122-03	RCA JACK, YELLOW	CN10
252122-01	RCA JACK, WHITE	CN4
252122-04	RCA JACK, BLACK	CN3
903326-08	8PIN SIL W/KEY	CN13
903345-17	HEADER 34PIN W/KEY	CN11
390248-01	RCA JACK, METAL	CN10
390248-01	RCA JACK, METAL	CN3,CN4

DIODES		
900850-01	1N4148	D501
390017-01	1N914	D501

FILTERS		
251842-02	EMI FILTER, 100pF	E511-E519,E421-E524,E611-E626
390275-02	EMI FILTER, 150pF	E402,E434,E532,E534
390297-01	EMI FILTER, 270pF	E305,E306
390297-04	EMI FILTER, 470pF	E415-E417,E425-E427,E441-E444,E520,E531,E533,E535-E538
390275-01	EMI FILTER, 6800pF	E302,E303,E411-E414,E421-E424
390297-05	EMI FILTER .01uF	E101,E401,E403-E408,E601,E602,E702-E704
252173-01	FERRITE BEAD RADIAL	E431-E433,R435
251878-02	LINE FILTER	LF1
252133-01	LONG FERRITE BEAD	FB802
903025-01	FERRITE BEAD AXIAL	E431-E433,E435

TRANSISTORS		
390254-01	JFET MPF102/PN4302	Q321,Q331
902658-01	NPN 2N3904	Q501,Q711
902707-01	PNP 2N3906	Q301,Q502,Q503

RESISTORS		
901600-36	1/2W CF, 1	R309
901600-50	1/2W CF, 4.7	R401,R405,R406,R408
901600-15	1/2W CF, 47	E501-E503
901550-64	1/4W CF, 10	R301,R302
901550-90	1/4W CF, 27	R101,R102
901550-56	1/4W CF, 47	R103-R107,R113
901550-94	1/4W CF, 68	E104,E105
901550-94	1/4W CF, 68	R111,R112,R114
901550-94	1/4W CF, 68	XR1
901550-49	1/4W CF, 100	R507
901550-89	1/4W CF, 150	FB101
901550-89	1/4W CF, 150	R409
901550-108	1/4W CF, 360	R321,R331
901550-57	1/4W CF, 390	R325,R335
901550-01	1/4W CF, 1K	R303-R305,R324,R334,R713
901550-23	1/4W CF, 2.7K	R307,R502
901550-19	1/4W CF, 4.7K	R201,R202,R402,R403,R503,R504
901550-20	1/4W CF, 10K	R306,R308,R322,R323,R332,R333,R339,R501,R505,R506
901550-22	1/4W CF, 47K	R712
901550-82	1/4W CF, 470K	R326,R336
901550-84	1/4W CF, 1M	R711
902410-11	RES PACK SIP PULLUP, 470 X 9	RP104
902410-08	RES PACK SIP PULLUP, 4.7K X 9	RP101,RP102,RP401
902410-07	RES PACK SIP PULLUP, 10K X 9	RP501
390227-03	RES PACK SIP SERIES, 22 X 5	RP103
390227-05	RES PACK SIP SERIES, 68 X 5	RP201,RP203
390227-06	RES PACK SIP SERIES, 47 X 5	RP402,RP403
901600-129	RES 1/2W CF, 5.1	R401,R405,R406,R408
390227-08	RES PACK SIP SERIES, 39 X 5	RP103
	NOT LOADED	RP105-RP111,RP405

MISCELLANEOUS		
904150-06	SOCKET, 40PIN DIP	U6-U8
251313-01	SOCKET, 48PIN DIP	U3-U5
904150-10	SOCKET, 64PIN DIP	U1
390185-01	SOCKET, 84PIN PLCC	U2
251313-02	SOCKET, 48PIN DIP	U3-U5
252344-01	OSCILLATOR, 28.37516NHz (PAL)	X1
325566-14	OSCILLATOR, 28.63636MHz (NTSC)	X1
312511-03	SCHEMATIC	

COMPONENT PARTS LIST
PCB ASSEMBLY RAM EXPANSION/CLOCK
PCB ASSEMBLY #312604-04, A501, REV. 6C

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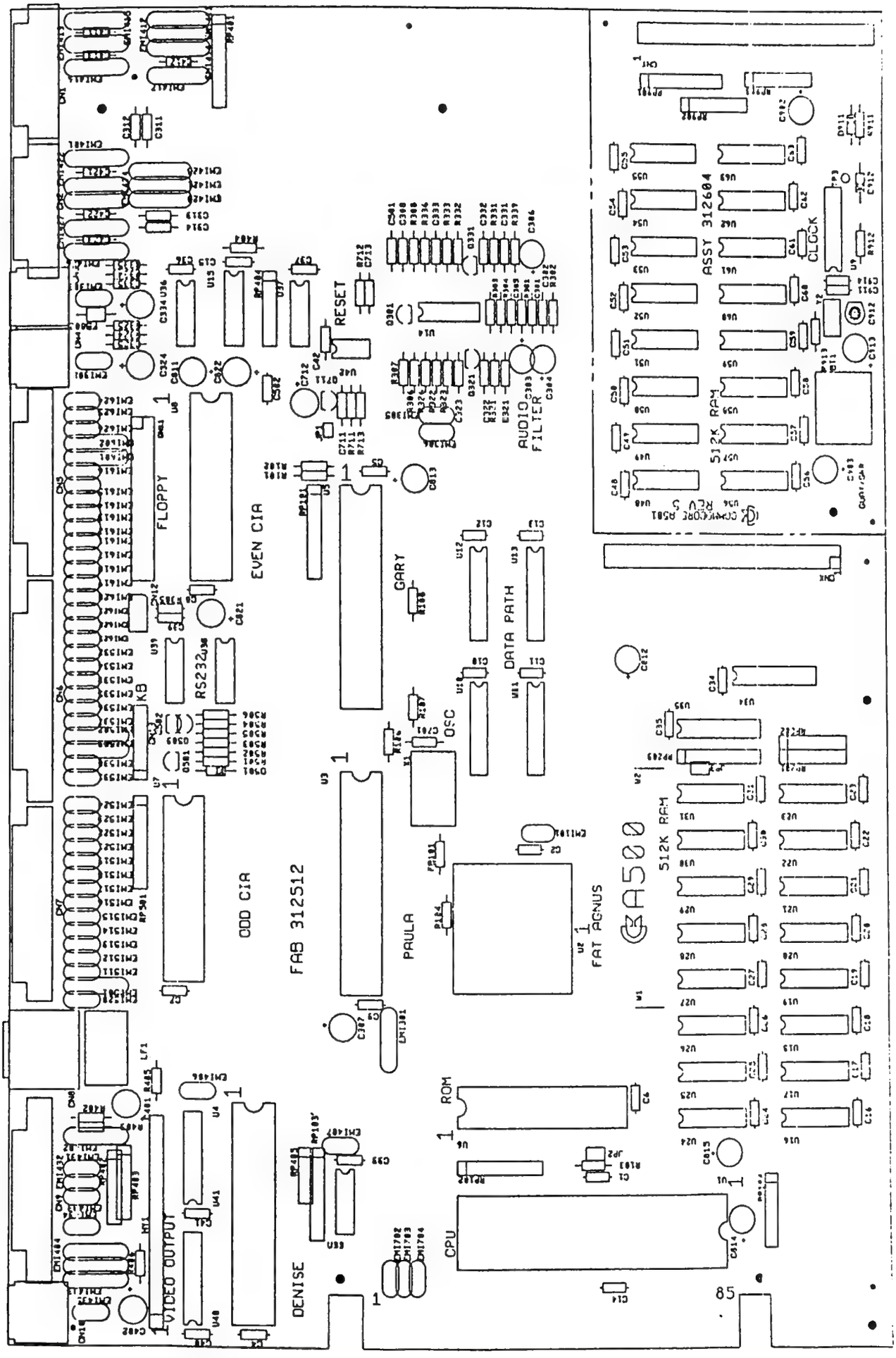
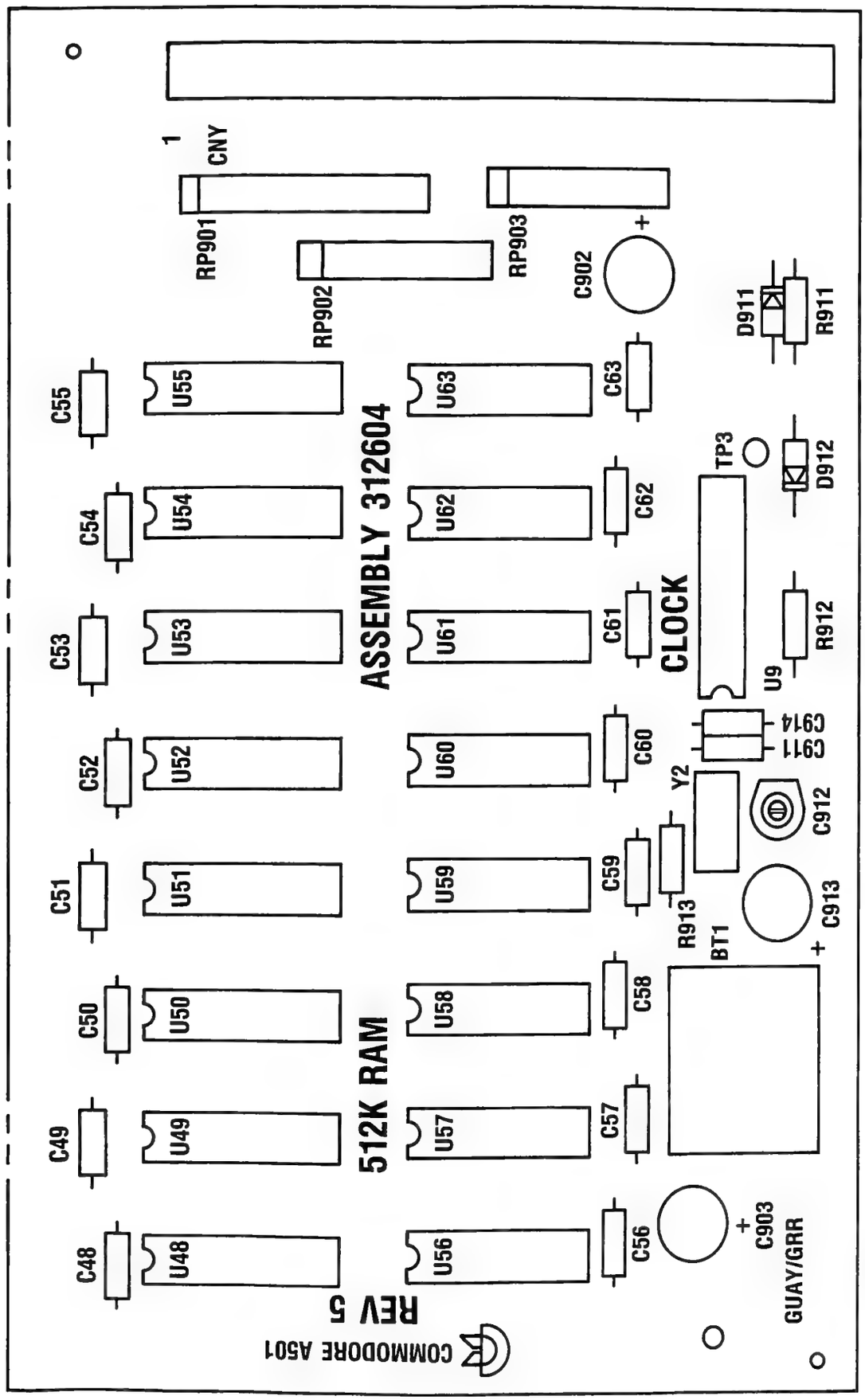
IC COMPONENTS		
318099-04	DRAM 256K X 4 120nS	U1-U4
318099-02	DRAM 256K X 4 100nS	U1-U4
318073-01	OKI MSM6242B REAL TIME CLOCK	U9
390392-01	TTL 74F27 TRIPLE 3-IN NOR	U13
390198-01	TTL 74F86 QUAD 2-IN XOR	U12
901521-33	TTL 74LS163 BINARY COUNTER	U11
RESISTORS		
901550-58	1/4W CF, 470	R911,R913
901550-20	1/4W CF, 10K	R912,R914,R915
390227-05	RES PACK SIP SERIES, 68 X 5	RP901-RP903,RP911
	NOT LOADED	RP912
CAPACITORS		
900462-21	MLC AXIAL NPO 22pF	C911
390082-01	MLC AXIAL Z5U .1uF	C9
390082-04	MLC AXIAL Z5U .33uF	C1-C4,C11-C13
251029-06	TRIMMER (YELLOW) 6.8-45pF	TC9
	NOT LOADED	C10
390101-02	ELECT ALUM RADIAL 100uF 16V	C902,C903
900410-13	ELECT TANTALUM RADIAL 4.7uF 16V	C913
390101-05	ELECT ALUM RADIAL 4.7uF 16V	C913

CONNECTORS		
380311-05	HEADER 56PIN FEMALE RA	CNY
DIODES		
900850-01	SWITCHING 1N4148	D912
390017-01	SWITCHING 1N914	D911
MISCELLANEOUS		
380393-01	BATTERY NICD VARTA 3/60DK, 3.6V 60MAH	BT9
900560-01	CRYSTAL WATCH STYLE, 32768Hz	Y9
312606-03	FABRICATION DRAWING	
312578-03	PCB ARTWORK	
312605-03	SCHEMATIC	



A500 Board Layout #312510, Rev. 5



NOTE: PN #312604-03 — A501 RAM/CLOCK PCB ASSEMBLY — INCLUDES SHIELDS AND INSULATION

BOARD LAYOUT
A501 RAM/CLOCK EXPANSION
PCB ASSEMBLY #312604-03

SECTION 5

SCHEMATICS

Jumpers and Stuff

REF	TYPE	DESCRIPTION	PAGE
JP1	BLOB	Keyboard Reset	7
JP2	BLOB	Memory Addr. C0 vs 00	2
JP3	BLOB	Int. Memory Ras0 vs 1	3
			4
TP1	POST	RTC Frequency Test	9
C912	TRIM	RTC Frequency Adjust	9
W1-2	0 Ohm	Ground Continuity FCC	8

Connectors

REF	TYPE	DESCRIPTION	PAGE
CN1	DB9P	Mouse/Joystick 1	2
CN2	DB9P	Mouse/Joystick 2	2
CN3	RCA-J	Right Audio Output	4
CN4	RCA-J	Left Audio Output	4
CN5	DB23S	External Floppy	7
CN6	DB25P	RS232 Serial Port	6
CN7	DB25S	Parallel Printer Port	6
CN8	SQ DIN	Power Supply Connector	8
CN9	DB23P	Video Output	5
CN10	RCA-J	Composite Video	5
CN11	DIL-34	Internal Floppy Signal	7
CN12	SIL-4	Internal Floppy Power	8
CN13	SIL-8	Keyboard Connector	6
P1	EDGE86	Expansion Connector	7
CNX	RA-56H	Mem. Exp. Main-Board	3
CNY	RA56-F	Mem. Exp. Sub-Board	9

ECO Log

ECO NUMBER	DESCRIPTION	DATE
870152	Additional Parts for FCC	05/12/87
870222	The "Transistor Fix"	06/16/87
870302	Change R1 resistor for FTZ	10/09/87
870207	More FCC Changes	09/04/87
880238	Add E Clock Termination	03/03/88

Signal Glossary

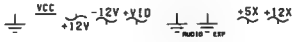
SIGNAL	DESCRIPTION (AREA)	PAGES
28MHZ	28.63636 MHz Master Clock	2
7MHZ	7.15909 MHz Processor Clock	2,5
A[23:1]	Processor Address Bus (68000)	2,3,7,9
ACK	Data Acknowledge (Parallel Port)	6
AS	Address Strobe (68000)	2,7
AUDIN	Audio Input (RS232 Port)	4,6
AUDOUT	Audio Output (RS232 Jack)	4,6
BERR	Bus Error (68000)	2,7
BG	Bus Grant (68000)	2,7
BGACK	Bus Grant Acknowledge (68000)	2,7
BLISS	Blitter Slowdown (Chips)	2
BLIT	Chip Memory Access (Chips)	2,7
BR	Bus Request (68000)	2,7
BUSY	Device Busy (Parallel Port)	6
CASL/U	Column Address Strobe (DRAM)	2,3,9
CCK/CCKQ	Color Clock / Quadrature (Chips)	2,4,7
CDAC	7.15909 MHz Quadrature Clock (Chips)	2,5,7
CHNG	Media Change (Floppy)	6,7
CLKRD/WR	Read-Time Clock Read / Write (RTC)	2,9
COMP	Monochrome Composite Video (Video)	5
CSYNC	Composite Sync (Video)	2,5
CTS	Clear to Send (RS232 Port)	6
D[15:0]	Processor Data Bus (68000)	2,3,6,7,9
DIR	Step Direction (Floppy)	6,7
DKRD	Disk Read Data (Floppy)	4,7
DKWD	Disk Write Data (Floppy)	4,7
DKWE	Disk Write Enable (Floppy)	4,7
DMAL	Chip DMA Request Line (Chips)	2,4
DRA[8:0]	DRAM Address Bus (DRAM)	2,3,9
DRD[15:0]	DRAM Data Bus (DRAM)	2,3,4,5,9
DSR	Data Set Ready (RS232 Port)	6
DTACK	Data Transfer Acknowledge (68000)	2,3,7
DTR	Data Terminal Ready (RS232 Port)	6
E	Peripheral Enable Clock (68000)	2,6,7
EXRAM	Expansion Memory Present	2,3,9
FC[2:0]	Function Code (68000)	2,7
FIRE0/1	Fire Button 0/1 (Joysticks)	2,5,6
HLT	Processor Halt (68000)	2,7
HSYNC	Horizontal Sync (Video)	2,5,6
INDEX	Index Pulse (Floppy)	6,7
INT[2,3,6]	Interrupt Request (Chips)	2,4,6,7
IORESET	I/O Reset	6,7
IPL[2:0]	Interrupt Priority Level (68000)	2,4,7
KBCLOCK	Keyboard Clock (Keyboard)	6
KBDATA	Keyboard Data (Keyboard)	6
KBRESET	Keyboard Reset (Keyboard)	6
LDS/UDS	Upper / Lower Data Strobes (68000)	2,7
LED	Power On LED / Audio Filter Disable	4,6

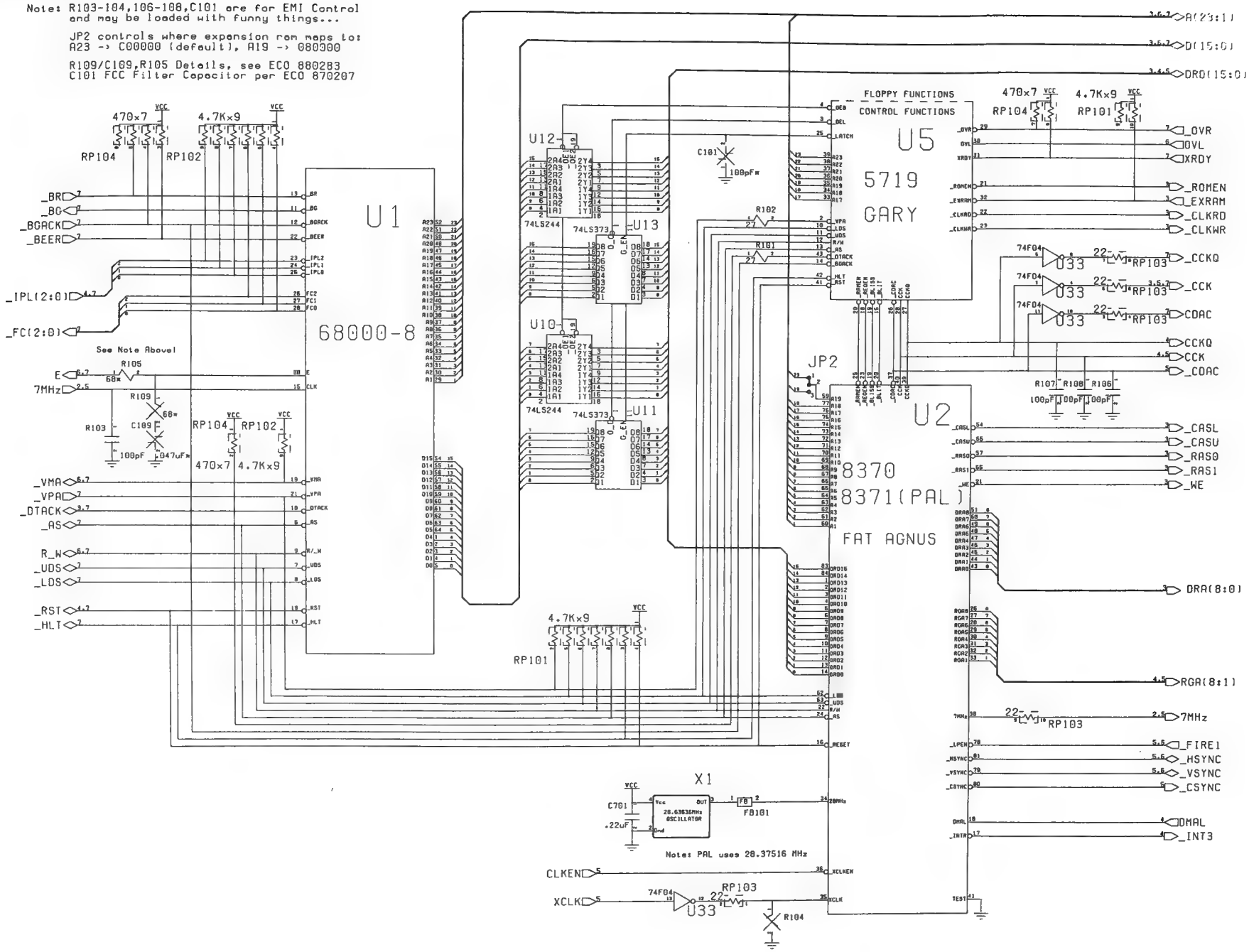
SIGNAL	DESCRIPTION (AREA)	PAGES
LEFT/RIGHT	Left Right Audio (Audio)	4
MTR	Motor On (Floppy)	4,6
MTR0	Motor On - Drive 0 (Floppy)	4,6,7
M0V/M0H	Mouse 0 Quadrature V/H (Joysticks)	5
M1V/M1H	Mouse 1 Quadrature V/H (Joysticks)	5
OVL	Overlay ROM over RAM	2,6
OVR	Override System Decoding	2,7
PIXELSW	Genlock Pixel Switch (Video)	5
POT0X/0Y	Pot Lines 0 X/Y (Joysticks)	4,5
POT1X/1Y	Pot Lines 1 X/Y (Joysticks)	4,5
POUT	Paper Out (Parallel Port)	6
PPD[7:0]	Parallel Port Data (Parallel Port)	6
RAMEN	RAM Enable (Chips)	2
REGEN	Chip Register Enable (Chips)	2
RAS0/1	Row Address Strobe (DRAM)	2,3,9
RDY	Drive Ready (Floppy)	6,7
RESET	General Reset	6,7
RGA[8:1]	Register Address Bus (Chips)	2,4,5
R/G/B	Red / Green / Blue (Video)	5
RI	Ring Indicate (RS232 Port)	6
ROMEN	ROM Enable (ROM)	2,3
RTS	Request to Send (RS232 Port)	6
RST	Processor Reset (68000)	2,4,7
RXD	Receive Data (RS232 Port)	4,6
RW	Processor Read/Write (68000)	2,6,7
SEL	Select (Parallel Port)	6
SEL[3:0]	Drive Select (Floppy)	4,6,7
SIDE	Side Select (Floppy)	6,7
STEP	Step In/Out Command (Floppy)	6,7
TRK0	Track Zero Sense (Floppy)	6,7
TXD	Transmit Data (RS232 Port)	4,6
VMA	Valid Memory Address (68000)	2,6,7
VPA	Valid Peripheral Address (68000)	2,7
VSYNC	Vertical Sync (Video)	2,5,6
WE	Write Enable (DRAM)	2,3,9
WPROT	Write Protect Sense (Floppy)	6,7
XCLK	External Genlock Clock (Video)	2,5
XCLKEN	External Clock Enable (Video)	2,5
XRDY	External Data Ready	2,5

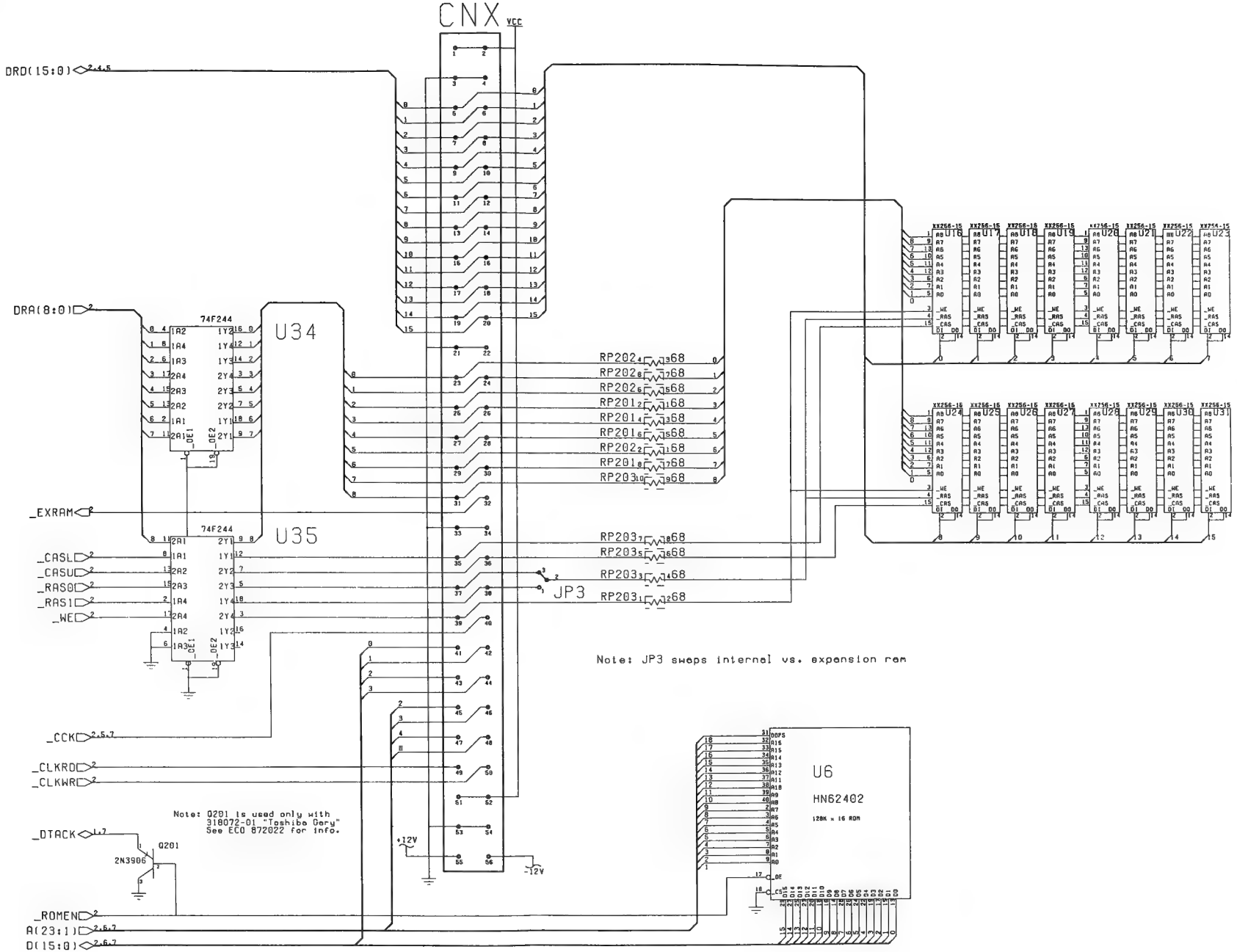
Key Components

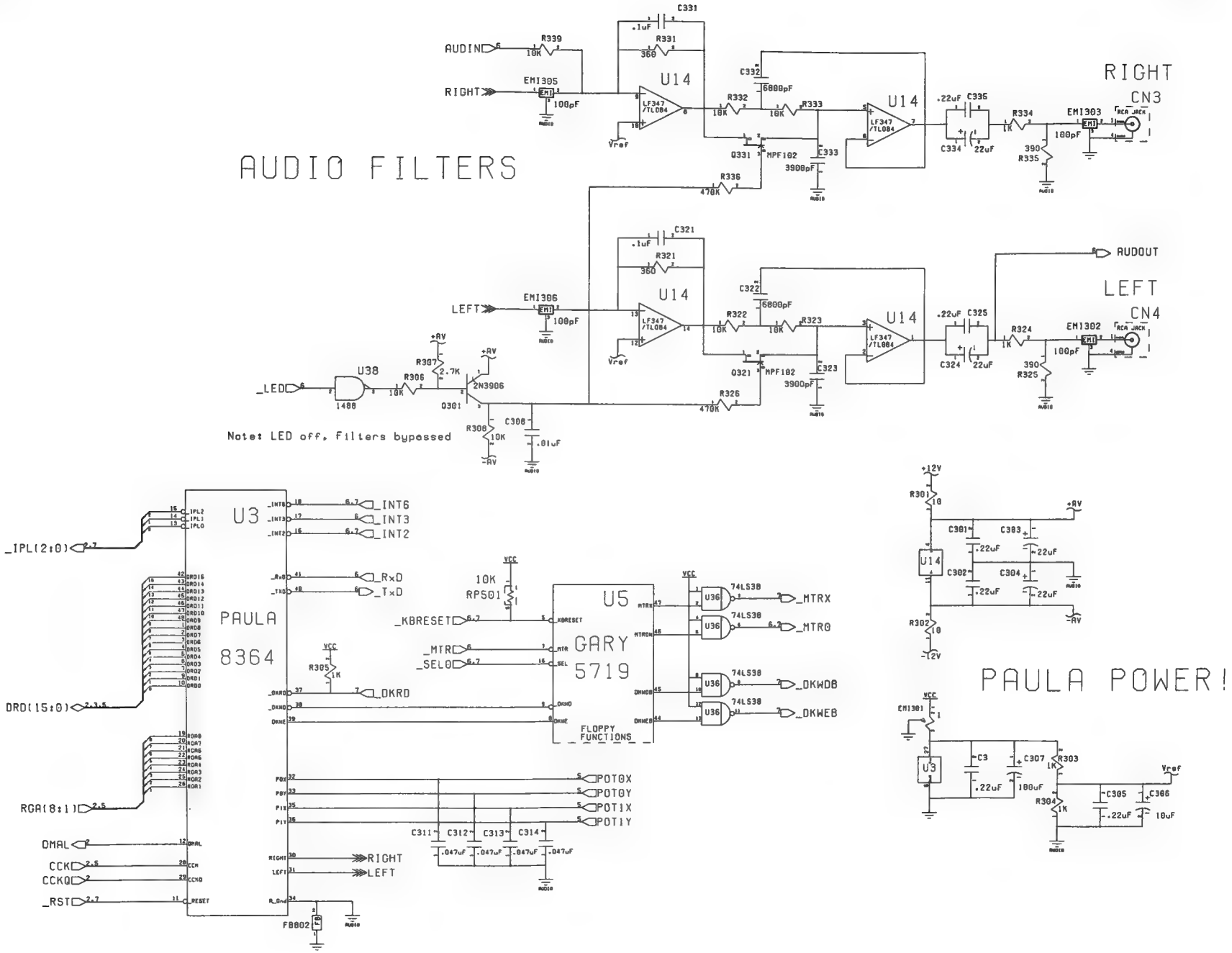
REF	CHIP	DESCRIPTION	PAGE
U1	68000	68000 Processor	2
U2	8370	Fat Agnus - NTSC	2
	8371	Fat Agnus - PAL	alt
	8372	Agnus HR	alt
U3	8364	Paula	4
U4	8362	Denise	5
	8373	Denise HR	alt
U5	5719	Gary	2,4
U6	asst	ROM 128Kx16, 200 nS	3
U7-8	8520	Amiga VIA, 1 MHz	6
U9	6242B	OKI Bus RTC	9
U14	LF347	BiMOS Op-Amp	4
	TL084	BiMOS Op-Amp	alt
U38	1488	EIA Line Driver	4
U39	1489	EIA Line Receiver	4
U42	NE555	Timer	7
U16-31	asst	DRAM 256Kx1, 150 nS	3
U48-63	asst	DRAM 256Kx1, 150 nS	9
X1	OSC	TTL 28.63636 MHz NTSC	2
	OSC	TTL 28.37512 MHz PAL	alt
Y2	XTAL	Watch Type 32768 Hz	9
HY1	asst	Video Hybrid	5

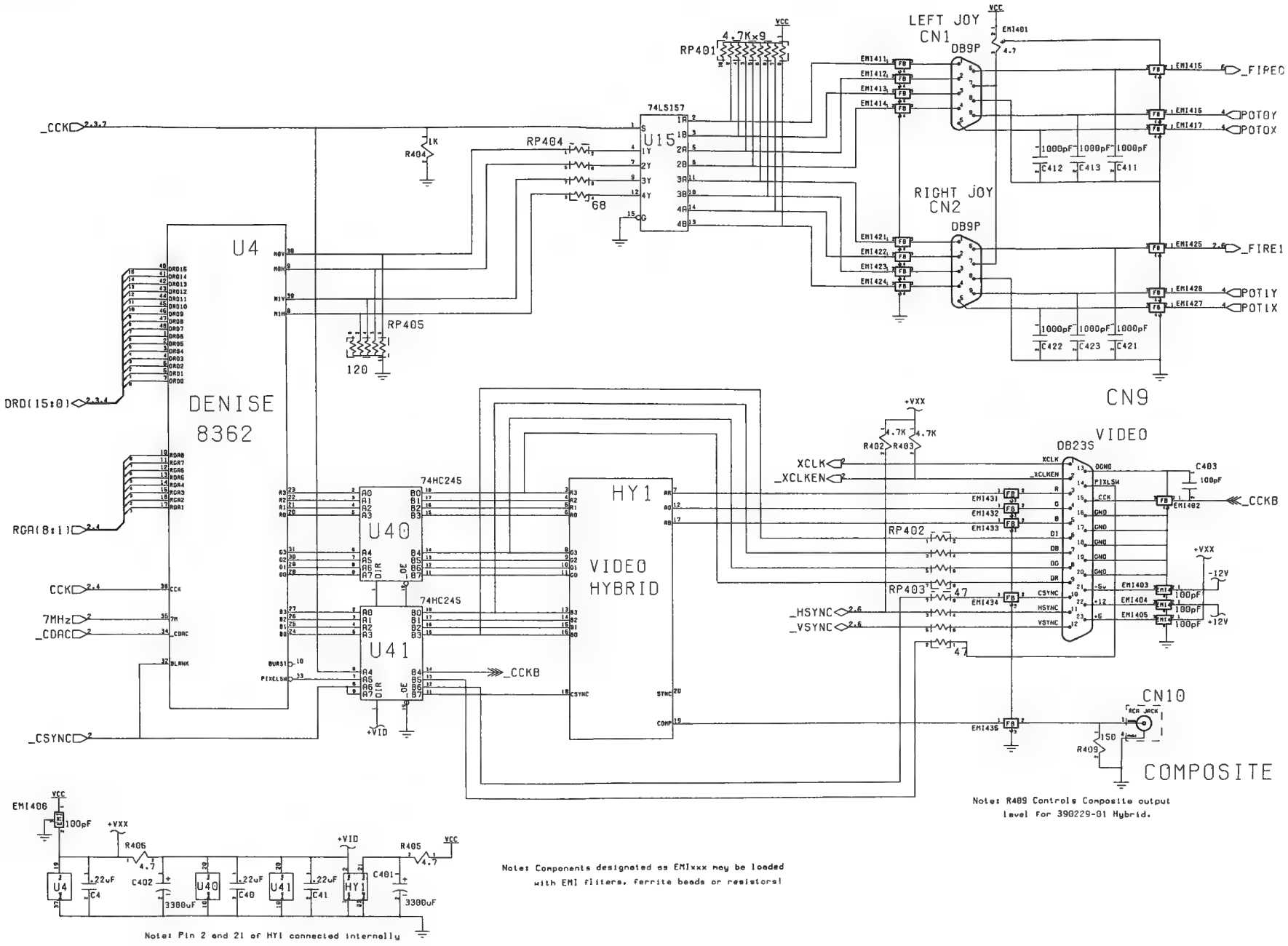
ATTEMPT TO FORCE NODE NUMBERS VIA SEQUENCE

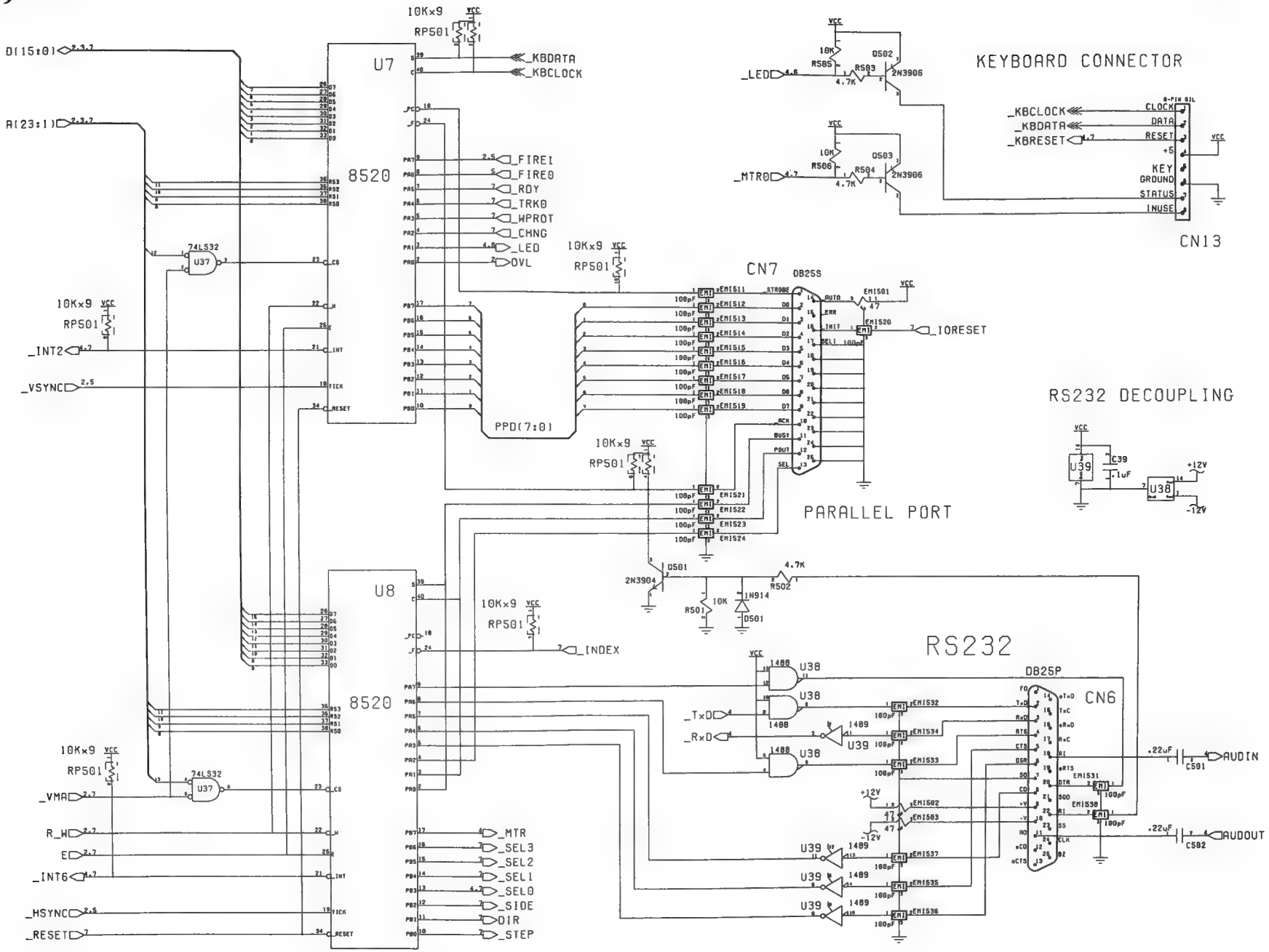


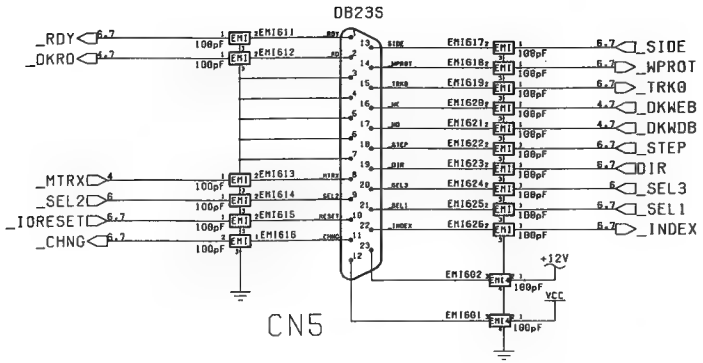

Note: R103-104,106-108,C101 are for EMI Control and may be loaded with funny things...
JP2 controls where expansion ram maps to: A23 -> C00000 (default), A19 -> 080000
R109/C109,R105 Details, see ECO 880283
C101 FCC Filter Capacitor per ECO 870207
U1
68000-8
U2
8370
8371(PAL)
FAT AGNUS
U5
5719
GARY
FLOPPY FUNCTIONS
CONTROL FUNCTIONS
U10
U11
U12
U13
74LS244
74LS373
74F04
U33
JP2
X1
28.63636MHz OSCILLATOR
Note: PAL uses 28.37516 MHz
See Note Above!
470x7
4.7Kx9
RP101
RP102
RP103
RP104
_BR
_BG
_BGACK
_BEER
_IPL(2:0)
_FC(2:0)
E
7MHz
_VMA
_VPA
_DTACK
_AS
R_W
_UDS
_LDS
_RST
_HLT
A(23:1)
D(15:0)
DRD(15:0)
_OVR
_OVL
XRDY
_ROMEN
_EXRAM
_CLKRD
_CLKWR
_CCKQ
_CCK
_CDAC
_CASL
_CASU
_RAS0
_RAS1
_WE
DRA(8:0)
RGA(8:1)
_FIRE1
_HSYNC
_VSYNC
_CSYNC
DMAL
_INT3
CLKEN
XCLK
R101
R102
R103
R104
R105
R106
R107
R108
R109
C101
C109
C701
FB101


CNX
VCC
DRD(15:0)
DRA(8:0)
74F244
U34
U35
_EXRAM
_CASL
_CASU
_RAS0
_RAS1
_WE
_CCK
_CLKRDO
_CLKWRO
_DTACK
Q201
2N3906
_ROMEN
A(23:1)
D(15:0)
RP2024 68
RP2028 68
RP2026 68
RP2012 68
RP2014 68
RP2016 68
RP2022 68
RP2018 68
RP2030 68
RP2037 68
RP2035 68
RP2033 68
RP2031 68
JP3
+12V
-12V
U6
HN62402
128K x 16 ROM
Note: JP3 swaps internal vs. expansion ram
Note: Q201 is used only with 318072-01 "Toshiba Gary" See ECO 872022 for info.


AUDIO FILTERS
AUDIN
RIGHT
LEFT
_LED
U14
U38
U3
U5
PAULA
8364
GARY
5719
FLOPPY
FUNCTIONS
PAULA POWER!
RIGHT
CN3
LEFT
CN4
AUDOUT
Q331
Q321
Q301
2N3906
MPF102
LF347
/TL084
1488
RPS01
10K
Vref
_IPL(2:0)
DRD(15:0)
RGA(8:1)
DMAL
CCK
CCKQ
_RST
_INT6
_INT3
_INT2
_RxD
_TxD
_DKRD
_DKWDB
_DKWEB
_MTRX
_MTR0
_KBRESET
_MTR
_SEL0
POT0X
POT0Y
POT1X
POT1Y
RIGHT
LEFT
FB802
74LS38
Note: LED off, Filters bypassed
Note: Ground interconnection near audio jacks.

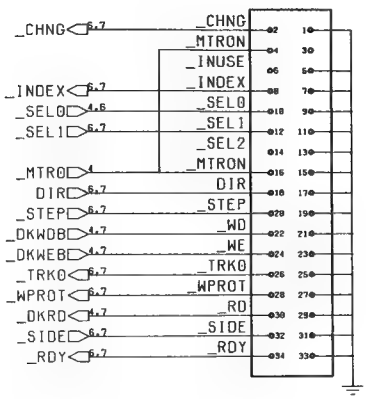

LEFT JOY
CN1
DB9P
RIGHT JOY
CN2
DB9P
CN9
RP401
4.7Kx9
74LS157
U15
RP404
68
R404
1K
RP405
120
U4
DENISE
8362
DRD(15:0)
RGA(8:1)
CCK
7MHz
_CDAC
_CSYNC
BLANK
BURST
PIXELSW
74HC245
U40
74HC245
U41
HY1
VIDEO
HYBRID
_CCKB
+VID
+VXX
R402
R403
4.7K
XCLK
_XCLKEN
_HSYNC
_VSYNC
RP402
RP403
47
DB23S
VIDEO
C403
100pF
_CCKB
-12V
+12V
CN10
RCA JACK
150
R409
COMPOSITE
_FIPEC
POTOY
POTOX
_FIRE1
POTIY
POTIX
1000pF
C412
C413
C411
C422
C423
C421
EMI406
100pF
R406
4.7
C402
3300uF
C40
C41
C401
R405
.22uF
C4
Note: Pin 2 and 21 of HY1 connected internally
Note: Components designated as EMIxxx may be loaded with EMI filters, ferrite beads or resistors!
Note: R409 Controls Composite output level for 390229-01 Hybrid.


KEYBOARD CONNECTOR
CN13
RS232 DECOUPLING
PARALLEL PORT
RS232
CN7
CN6
U7
U8
8520
74LS32
U37
U38
U39
RP501
10Kx9
PPD(7:0)
_KBDATA
_KBCLOCK
_KBRESET
_LED
_MTR0
_FIRE1
_FIRE0
_RDY
_TRK0
_WPROT
_CHNG
_OVL
_IORESET
_INT2
_VSYNC
_INDEX
_VMA
R_W
E
_INT6
_HSYNC
_RESET
_MTR
_SEL3
_SEL2
_SEL1
_SEL0
_SIDE
DIR
_STEP
_TxD
_RxD
AUDIN
AUDOUT
+12V
-12V
VCC
2N3906
2N3904
1N914
Note: EMI501-503 are loaded with 47 Ohm 1/2 W resistors

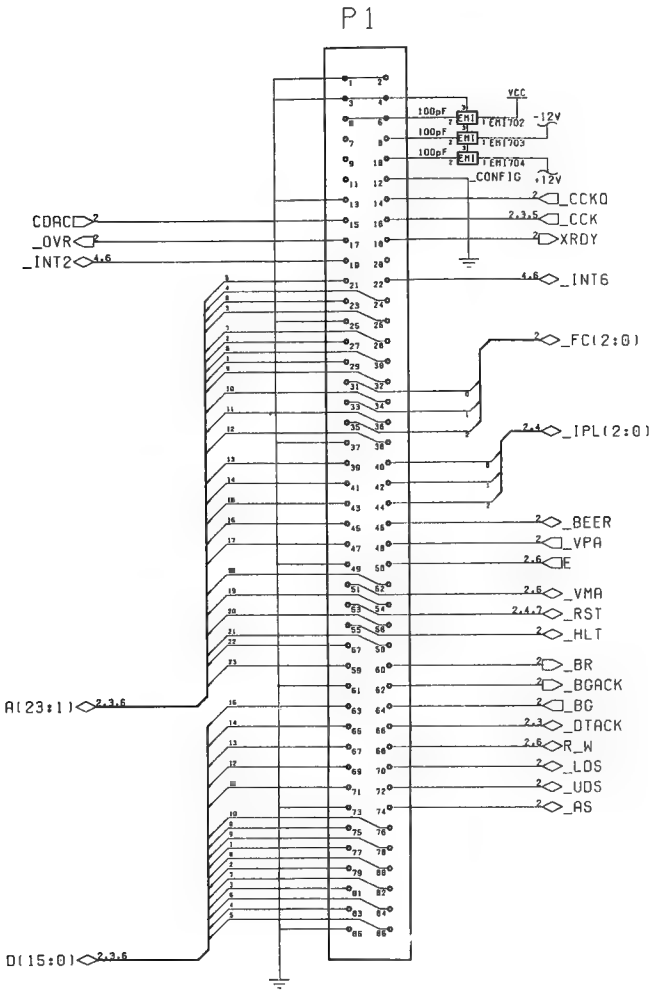


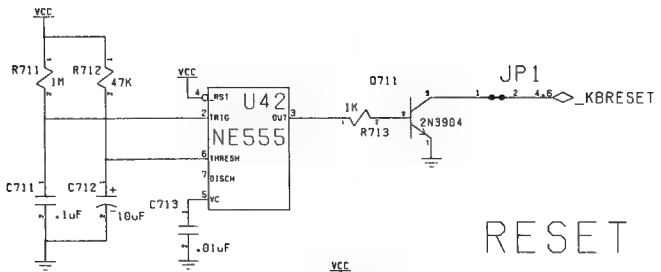
EXTERNAL FLOPPY

INTERNAL FLOPPY

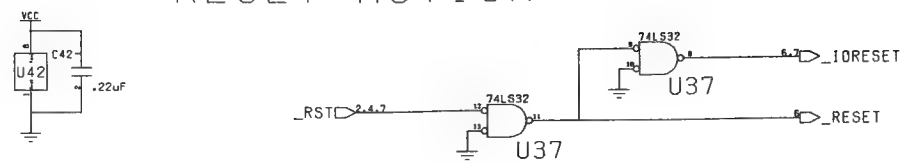


EXPANSION

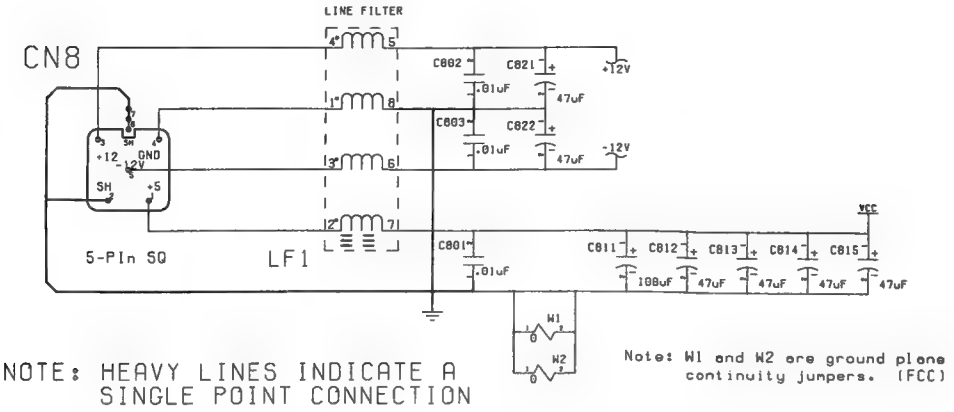




RESET ACTION



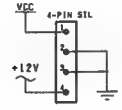
POWER INPUT



NOTE: HEAVY LINES INDICATE A SINGLE POINT CONNECTION

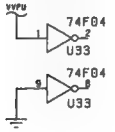
Note: W1 and W2 are ground plane continuity jumpers. (FCC)

FLOPPY POWER

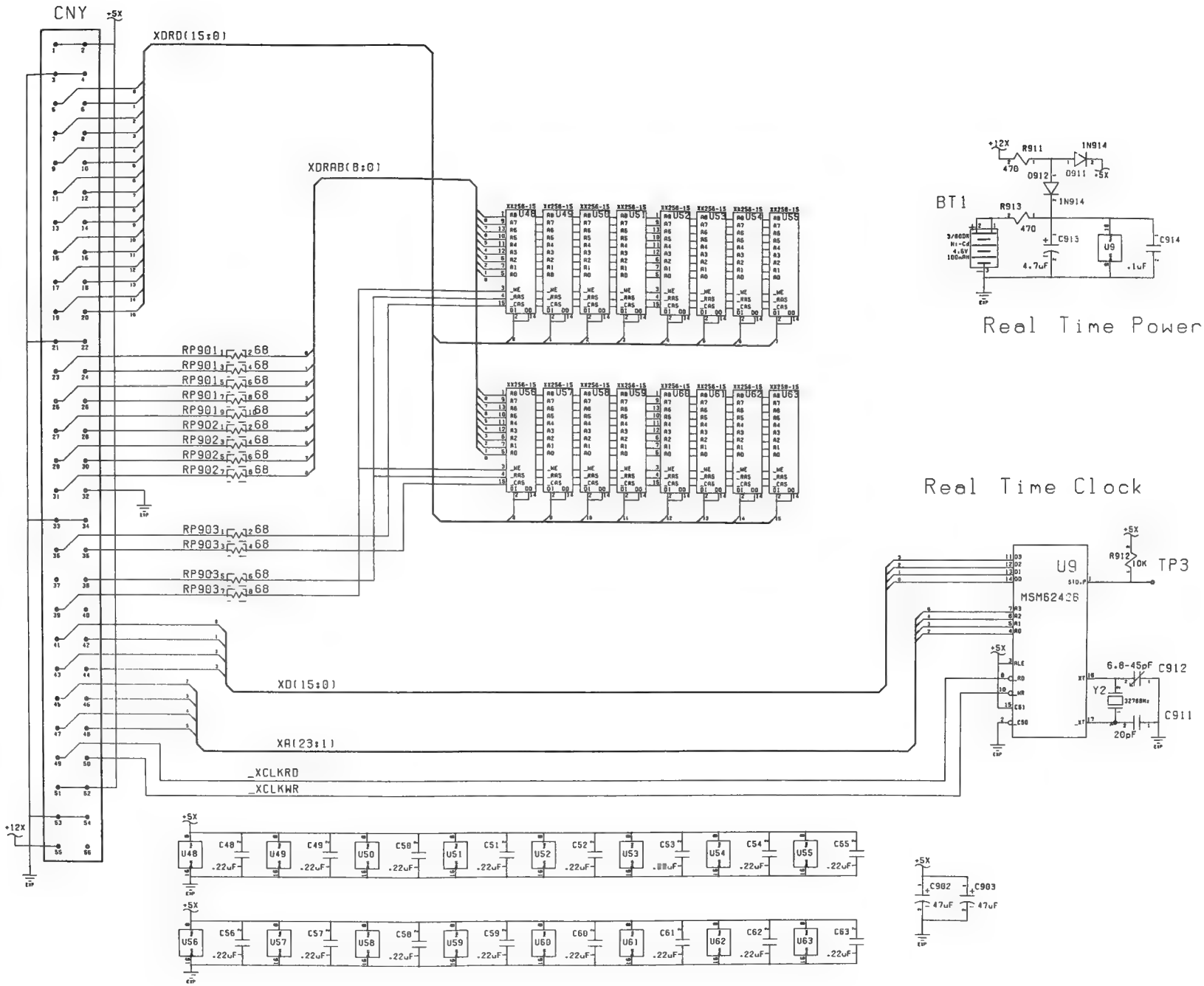


CN12

SPARES



DECOUPLING


CNY
+5X
XDRD(15:0)
XDRAB(8:0)
RP901 68
RP902 68
RP903 68
XD(15:0)
XA(23:1)
_XCLKRD
_XCLKWR
+12X
U48
U49
U50
U51
U52
U53
U54
U55
U56
U57
U58
U59
U60
U61
U62
U63
.22uF
Real Time Power
BT1
R911
1N914
470
D912
D911
R913
C913
4.7uF
C914
.1uF
Real Time Clock
U9
MSM62436
R912
10K
TP3
Y2
32768Hz
6.8-45pF C912
C911
20pF
C902
C903
47uF

Jumpers and Stuff

REF	TYPE	DESCRIPTION	PAGE
JP1	BLOB	Keyboard Reset	7
JP2	BLOB	Memory Addr. C0 vs 08	2
JP3	BLOB	Expansion RAS Select	3
JP4	BLOB	NTSC/PAL Selection	2
JP5	BLOB	Genlock Clock Select	2
JP6	BLOB	7MHz Clock Option	7
JP7	BLOB	Expansion/Tick Option	3/6
JP8	BLOB	Light Pen Port Select	6
JP10	BLOB	RS232 Audio I/O Cutout	4
JP11	BLOB	TTL vs RS170 Comp Sync	5

Connectors

REF	TYPE	DESCRIPTION	PAGE
CN1	DB9P	Mouse/Joystick 1	2
CN2	DB9P	Mouse/Joystick 2	2
CN3	RCA-J	Right Audio Output	4
CN4	RCA-J	Left Audio Output	4
CN5	DB23S	External Floppy	7
CN6	DB25P	RS232 Serial Port	6
CN7	DB25S	Parallel Printer Port	6
CN8	SQ DIN	Power Supply Connector	8
CN9	DB23P	Video Output	5
CN10	RCA-J	Composite Video	5
CN11	DIL-34	Internal Floppy Signal	7
CN12	SIL-4	Internal Floppy Power	E
CN13	SIL-8	Keyboard Connector	E
P1	EDGE86	Expansion Connector	7
CNX	RA-56H	Mem. Exp. Main-Board	3

ECO Log

ECO NUMBER	DESCRIPTION	DATE
880283	Add E Clock Termination	03/03/89

Signal Glossary

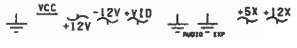
SIGNAL	DESCRIPTION (AREA)	PAGES
28MHZ	28.63636 MHz Master Clock	2
7MHZ	7.15909 MHz Processor Clock	2,5
A[23:1]	Processor Address Bus (68000)	2,3,7
ACK	Data Acknowledge (Parallel Port)	6
AS	Address Strobe (68000)	2,7
AUDIN	Audio Input (RS232 Port)	4,6
AUDOUT	Audio Output (RS232 Jack)	4,6
BEER	Bus Error (68000)	2,7
BG	Bus Grant (68000)	2,7
BGACK	Bus Grant Acknowledge (68000)	2,7
BLISS	Blitter Slowdown (Chips)	2
BLIT	Chip Memory Access (Chips)	2,7
BR	Bus Request (68000)	2,7
BUSY	Device Busy (Parallel Port)	6
CASL/U	Column Address Strobe (DRAM)	2,3
CCK/CCKQ	Color Clock / Quadrature (Chips)	2,4,7
CDAC	7.15909 MHz Quadrature Clock (Chips)	2,5,7
CHNG	Media Change (Floppy)	6,7
CLKRD/WR	Real-Time Clock Read / Write (RTC)	2,9
COMP	Monochrome Composite Video (Video)	5
CSYNC	Composite Sync (Video)	2,5
CTS	Clear to Send (RS232 Port)	6
D[15:0]	Processor Data Bus (68000)	2,3,6,7
DIR	Step Direction (Floppy)	6,7
DKRD	Disk Read Data (Floppy)	4,7
DKWD	Disk Write Data (Floppy)	4,7
DKWE	Disk Write Enable (Floppy)	4,7
DMAL	Chip DMA Request Line (Chips)	2,4
DRA[8:0]	DRAM Address Bus (DRAM)	2,3
DRD[15:0]	DRAM Data Bus (DRAM)	2,3,4,5
DSR	Data Set Ready (RS232 Port)	6
DTACK	Data Transfer Acknowledge (68000)	2,3,7
DTR	Data Terminal Ready (RS232 Port)	6
E	Peripheral Enable Clock (68000)	2,6,7
EXTICK	Expansion Present / RTC Tick	2,3
FC[2:0]	Function Code (68000)	2,7
FIRE0/1	Fire Button 0/1 (Joysticks)	2,5,6
HLT	Processor Halt (68000)	2,7
HSYNC	Horizontal Sync (Video)	2,5,6
INDEX	Index Pulse (Floppy)	6,7
INT[2,3,6]	Interrupt Request (Chips)	2,4,6,7
IORESET	I/O Reset	6,7
IPL[2:0]	Interrupt Priority Level (68000)	2,4,7
KBCLOCK	Keyboard Clock (Keyboard)	6
KBDATA	Keyboard Data (Keyboard)	6
KBRESET	Keyboard Reset (Keyboard)	6
LDS/UDS	Upper / Lower Data Strobes (68000)	2,7
LED	Power On LED / Audio Filter Disable	4,6
LEFT/RIGHT	Left Right Audio (Audio)	4

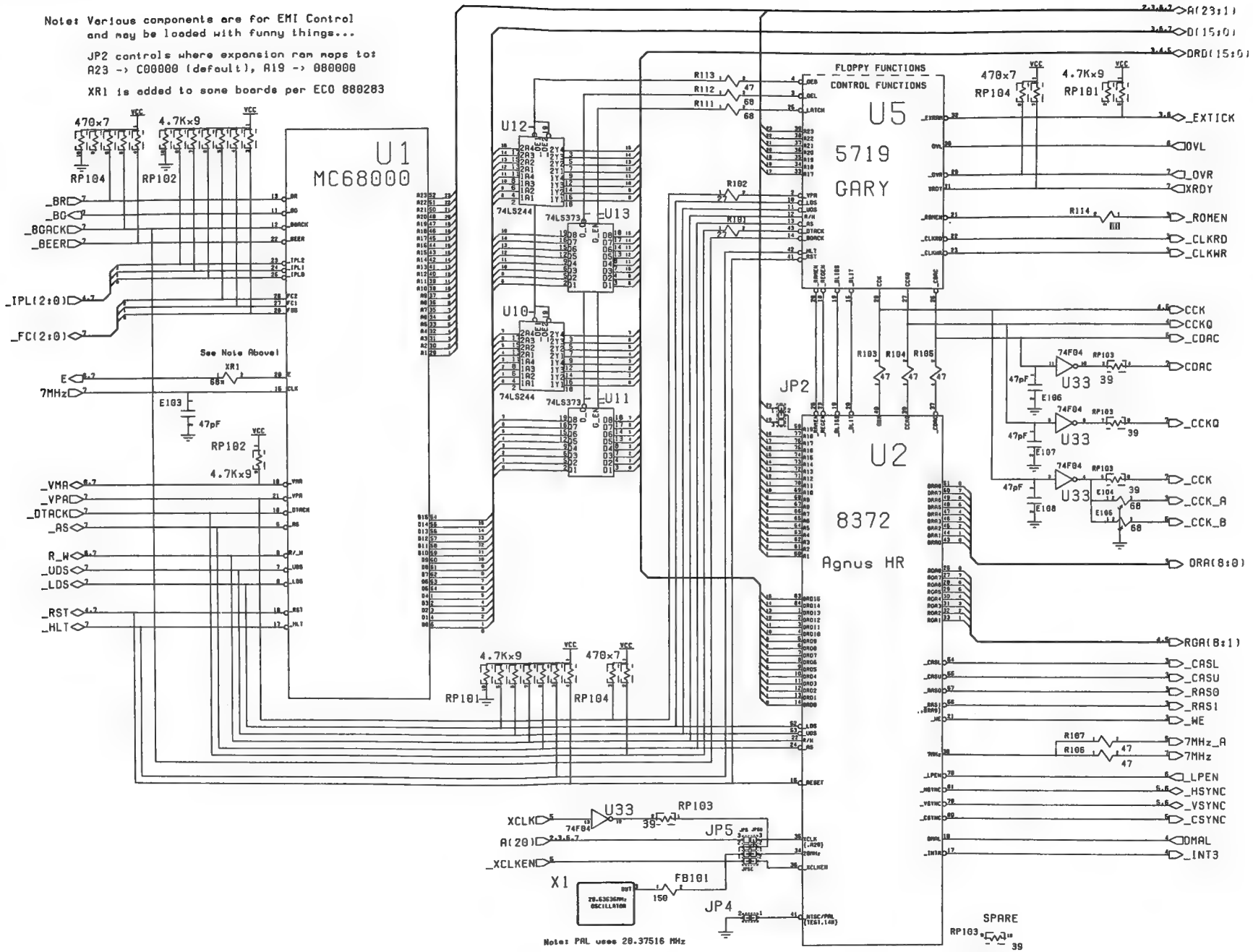
SIGNAL	DESCRIPTION (AREA)	PAGES
LPEN	Light Pen Trigger (Joysticks)	2,6
MTR	Motor On (Floppy)	4,6
MTR0	Motor On - Drive 0 (Floppy)	4,6,7
M0V/M0H	Mouse 0 Quadrature V/H (Joysticks)	5
M1V/M1H	Mouse 1 Quadrature V/H (Joysticks)	5
OVL	Overlay ROM over RAM	2,6
OVR	Override System Decoding	2,7
PIXELSW	Genlock Pixel Switch (Video)	5
POT0X/0Y	Pot Lines 0 X/Y (Joysticks)	4,5
POT1X/1Y	Pot Lines 1 X/Y (Joysticks)	4,5
POUT	Paper Out (Parallel Port)	6
PPD[7:0]	Parallel Port Data (Parallel Port)	6
RAMEN	RAM Enable (Chips)	2
REGEN	Chip Register Enable (Chips)	2
RAS0/1	Row Address Strobe (DRAM)	2,3
RDY	Drive Ready (Floppy)	6,7
RESET	General Reset	6,7
RGA[8:1]	Register Address Bus (Chips)	2,4,5
R/G/B	Red / Green / Blue (Video)	5
RI	Ring Indicate (RS232 Port)	6
ROMEN	ROM Enable (ROM)	2,3
RTS	Request to Send (RS232 Port)	6
RST	Processor Reset (68000)	2,4,7
RXD	Receive Data (RS232 Port)	4,6
RW	Processor Read/Write (68000)	2,6,7
SEL	Select (Parallel Port)	6
SEL[3:0]	Drive Select (Floppy)	4,6,7
SIDE	Side Select (Floppy)	6,7
STEP	Step In/Out Command (Floppy)	6,7
TRK0	Track Zero Sense (Floppy)	6,7
TXD	Transmit Data (RS232 Port)	4,6
VMA	Valid Memory Address (68000)	2,6,7
VPA	Valid Peripheral Address (68000)	2,7
VSYNC	Vertical Sync (Video)	2,5,6
WE	Write Enable (DRAM)	2,3
WPROT	Write Protect Sense (Floppy)	6,7
XCLK	External Genlock Clock (Video)	2,5
XCLKEN	External Clock Enable (Video)	2,5
XRDY	External Data Ready	2,5

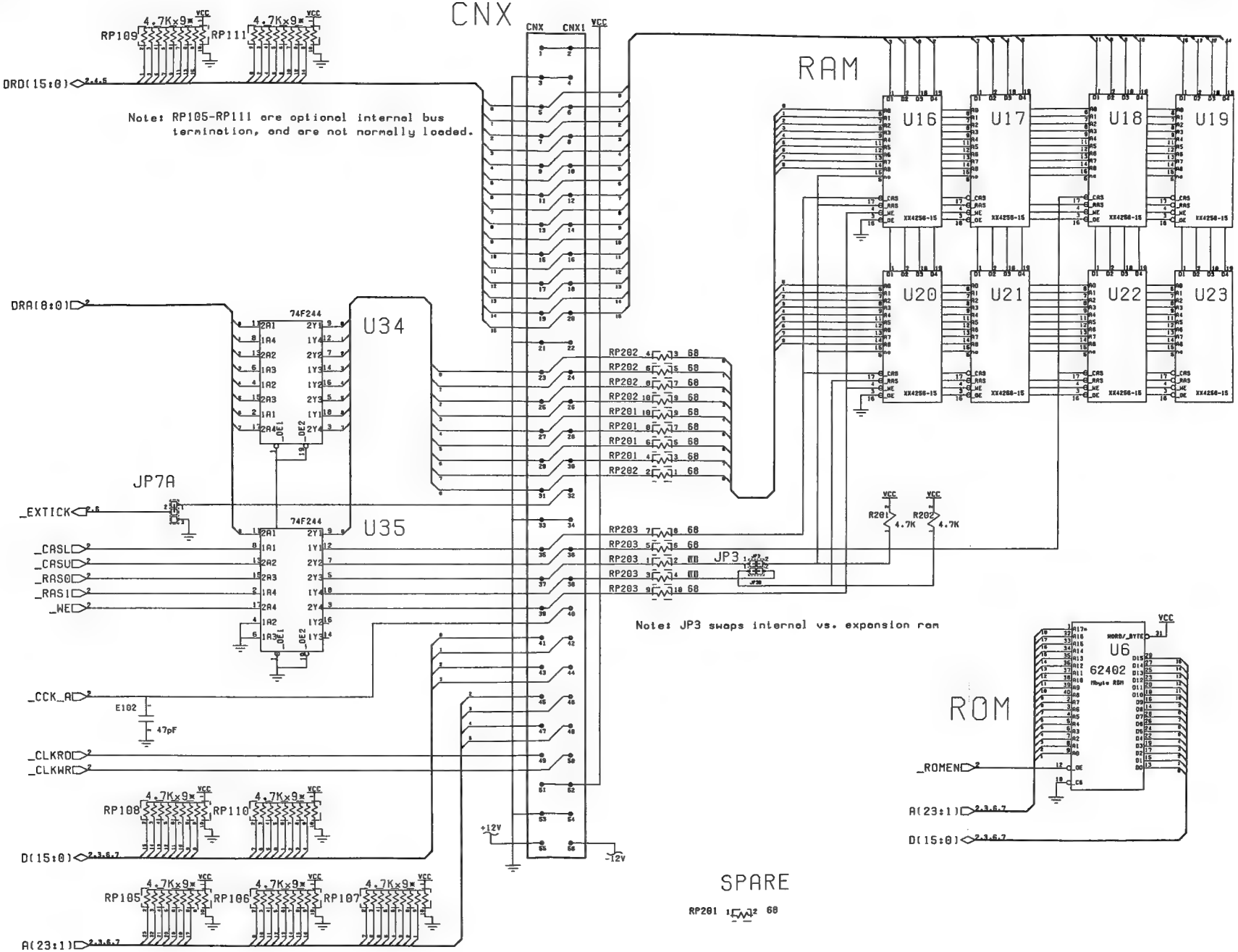
Key Components

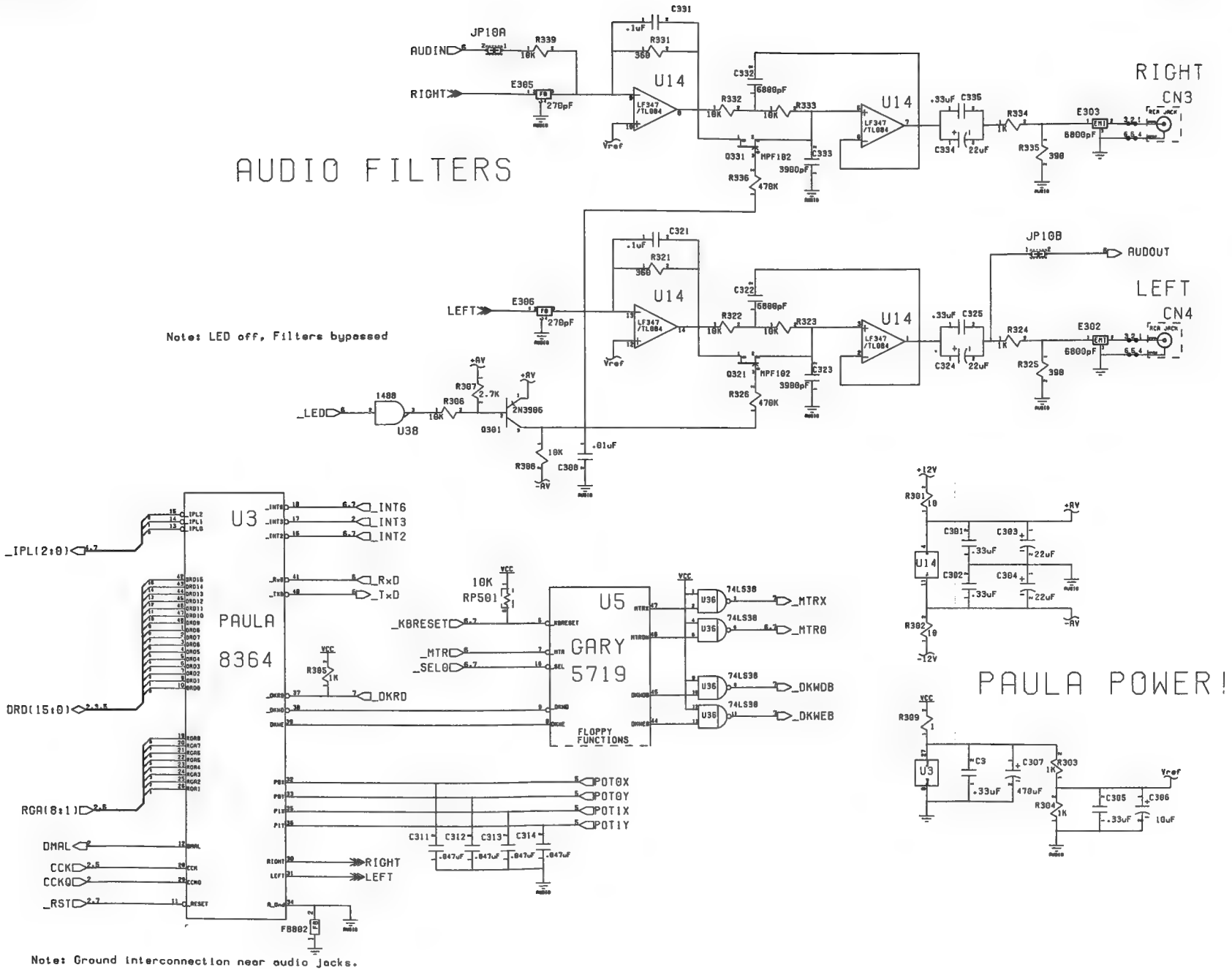
REF	CHIP	DESCRIPTION	PAGE
U1	68000	68000 Processor	2
U2	8370	Fat Agnus - NTSC	2
	8371	Fat Agnus - PAL	alt
	8372	Agnus HR	alt
U3	8364	Paula	4
U4	8362	Denise	5
	8373	Denise HR	alt
U5	5719	Gary	2,4
U6	asst	ROM 128Kx16, 200 nS	3
U7-8	8520	Amiga VIA, 1 MHz	6
U14	LF347	BiMOS Op-Amp	4
	TL084	BiMOS Op-Amp	alt
U38	1488	EIA Line Driver	4
U39	1489	EIA Line Receiver	4
U42	NE555	Timer	7
U16-19	asst	DRAM 1Mx1, 150 nS	3
U20-23	asst	DRAM 1Mx1, 150 nS	9
X1	OSC	TTL 28.63636 MHz NTSC	2
	OSC	TTL 28.37512 MHz PAL	alt
HY1	asst	Video Hybrid	5

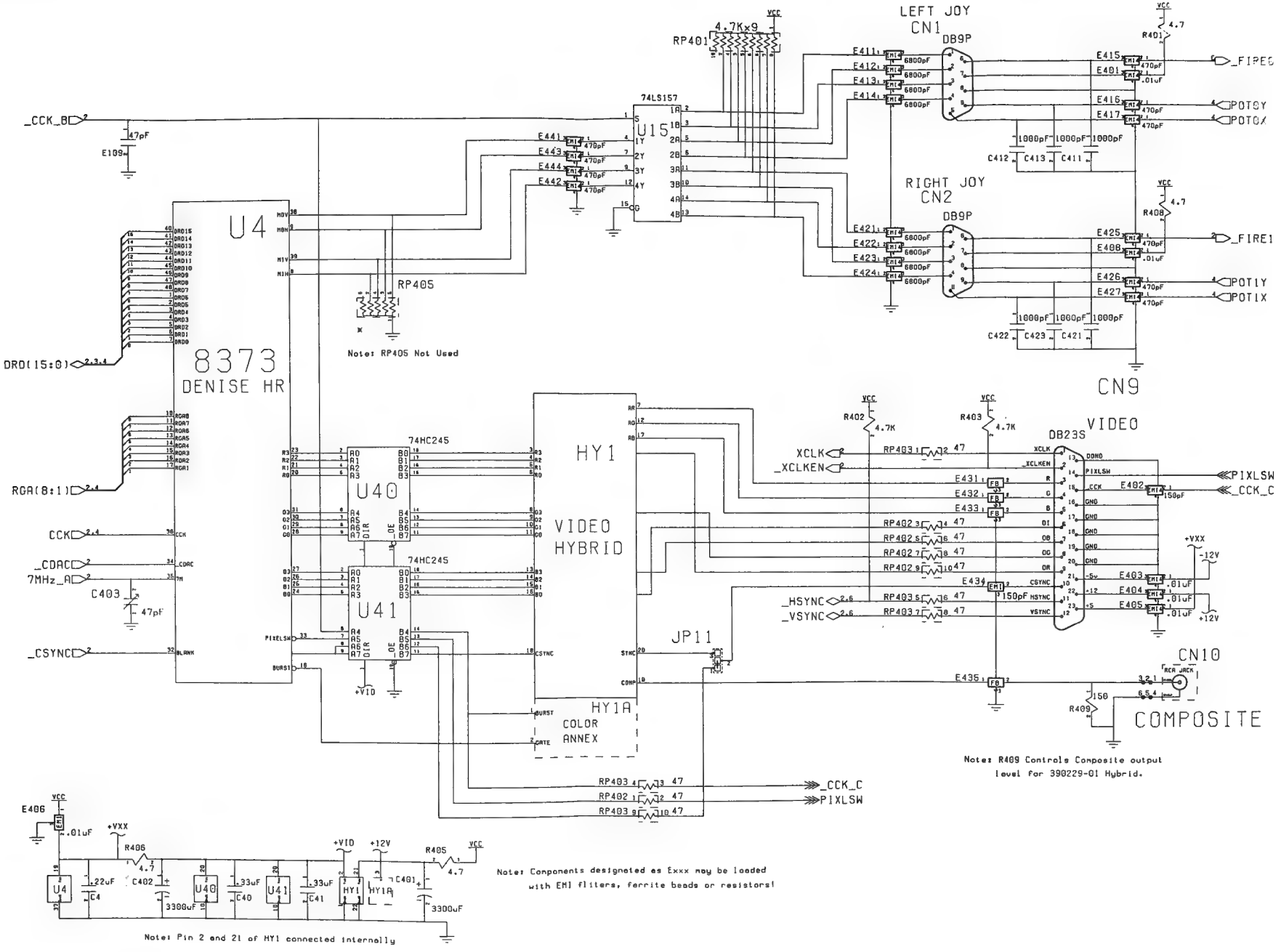
ATTEMPT TO FORCE NODE NUMBERS VIA SEQUENCE

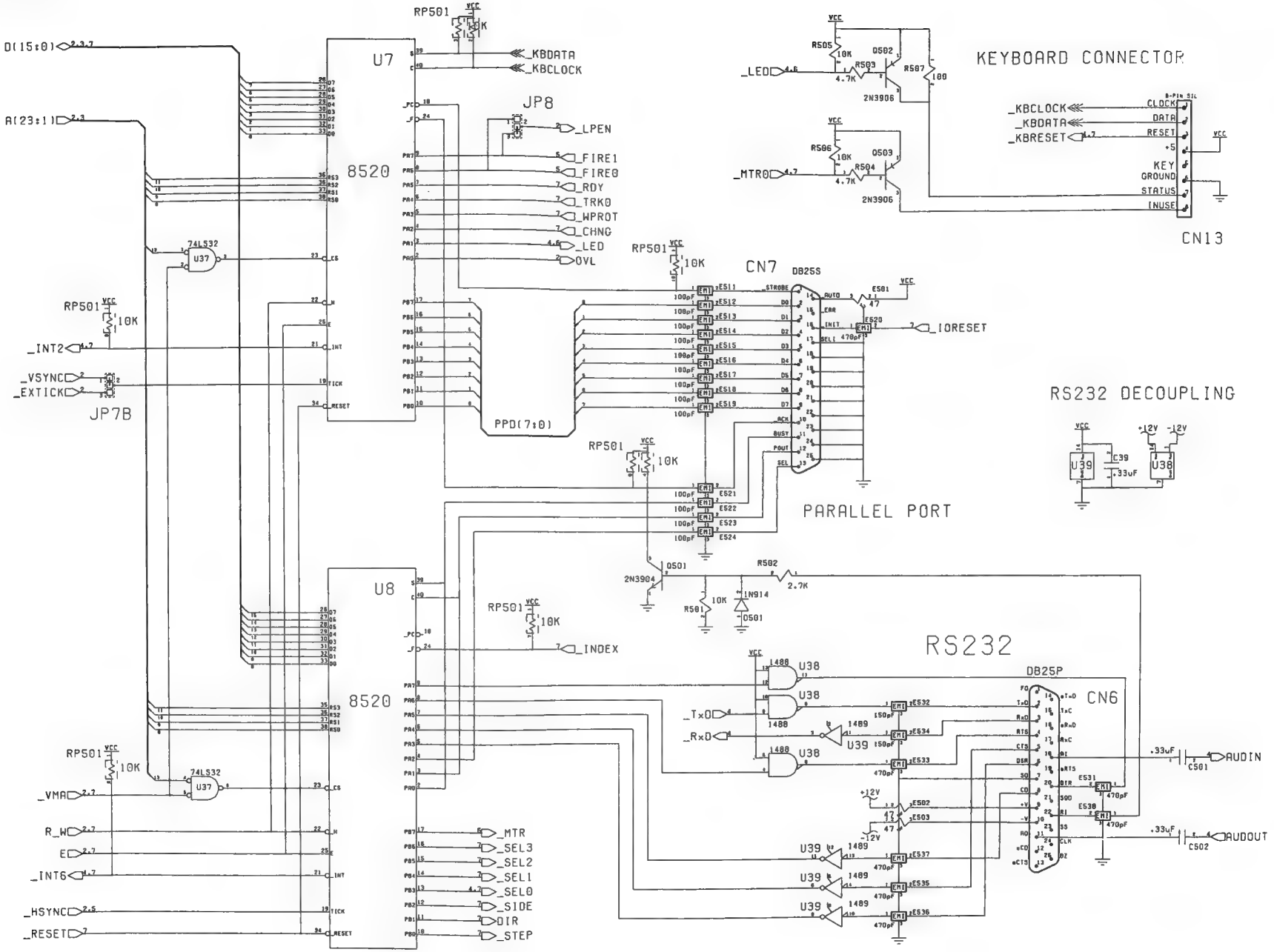



Note: Various components are for EMI Control and may be loaded with funny things...
JP2 controls where expansion ram maps to: A23 -> C00000 (default), A19 -> 080000
XR1 is added to some boards per ECO 880283
U1
MC68000
U2
8372
Agnus HR
U5
5719
GARY
FLOPPY FUNCTIONS
CONTROL FUNCTIONS
U10
U11
U12
U13
74LS244
74LS373
74F04
RP101
RP102
RP103
RP104
470x7
4.7Kx9
See Note Above!
XR1
E103
47pF
JP2
JP4
JP5
X1
FB101
150
SPARE
Note: PAL uses 28.37516 MHz
A(23:1)
D(15:0)
DRD(15:0)
_EXTICK
_OVL
_OVR
_XRDY
_ROMEN
_CLKRD
_CLKWR
_BR
_BG
_BGACK
_BEER
_IPL(2:0)
_FC(2:0)
E
7MHz
_VMA
_VPA
_DTACK
_AS
R_W
_UDS
_LDS
_RST
_HLT
CCK
CCKQ
_CDAC
_CCKQ
_CCK
_CCK_A
_CCK_B
DRA(8:0)
RGA(8:1)
_CASL
_CASU
_RAS0
_RAS1
_WE
7MHz_A
7MHz
_LPEN
_HSYNC
_VSYNC
_CSYNC
_DMAL
_INT3
XCLK
A(20)
_XCLKEN

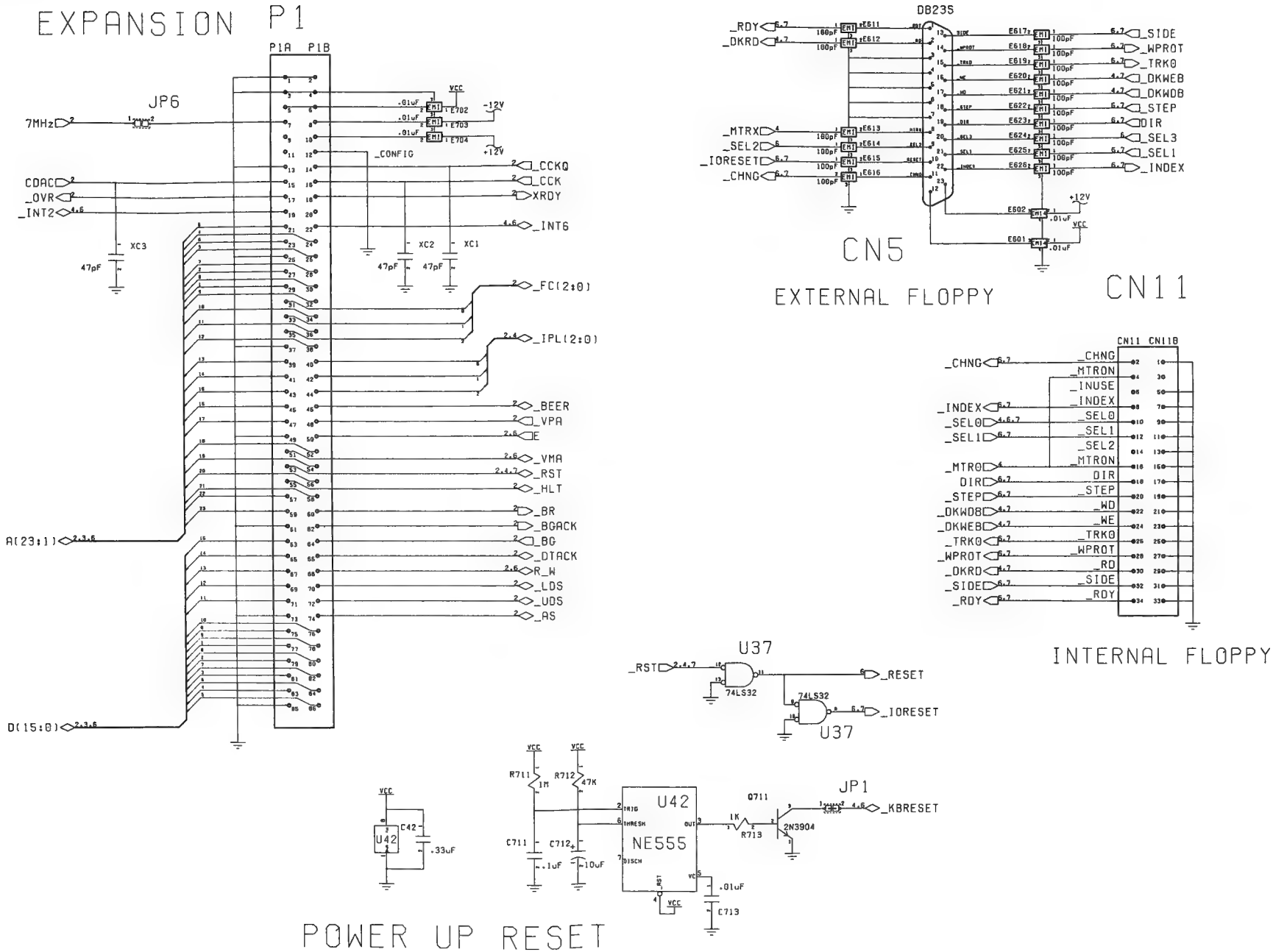

CNX
RAM
ROM
SPARE
U34
U35
U6
JP7A
JP3
RP109
RP111
RP108
RP110
RP105
RP106
RP107
RP202
RP201
RP203
R201
R202
E102
47pF
4.7K×9
74F244
62402
DRD(15:0)
DRA(8:0)
_EXTICK
_CASL
_CASU
_RAS0
_RAS1
_WE
_CCK_A
_CLKRD
_CLKWR
D(15:0)
A(23:1)
_ROMEN
+12V
-12V
Note: RP105-RP111 are optional internal bus termination, and are not normally loaded.
Note: JP3 swaps internal vs. expansion ram


AUDIO FILTERS
JP10A
AUDIN
RIGHT
E305
R339
10K
C331
.1uF
R331
360
U14
LF347
/TL084
Vref
C332
6800pF
R332
10K
R333
10K
Q331
MPF102
C333
3900pF
R336
470K
.33uF C335
C334
22uF
R334
1K
R335
390
E303
6800pF
RIGHT
CN3
RCA JACK
Note: LED off, Filters bypassed
LEFT
E306
270pF
C321
.1uF
R321
360
C322
6800pF
R322
10K
R323
10K
Q321
MPF102
C323
3900pF
R326
470K
C324
22uF
R324
1K
R325
390
E302
6800pF
JP10B
AUDOUT
LEFT
CN4
_LED
1488
U38
R307
2.7K
R306
10K
Q301
2N3906
+RV
-RV
R308
10K
C308
.01uF
U3
PAULA
8364
_IPL(2:0)
DRD(15:0)
RGA(8:1)
DMAL
CCK
CCKQ
_RST
_INT6
_INT3
_INT2
RxD
TxD
_DKRD
RIGHT
LEFT
FB802
U5
GARY
5719
10K
RP501
_KBRESET
_MTR
_SEL0
R305
1K
74LS38
_MTRX
_MTR0
_DKWDB
_DKWEB
FLOPPY
FUNCTIONS
POT0X
POT0Y
POT1X
POT1Y
C311
C312
C313
C314
.047uF
+12V
-12V
R301
10
R302
10
C301
C303
.33uF
22uF
C302
C304
.33uF
22uF
PAULA POWER!
R309
1
C3
.33uF
C307
470uF
R303
1K
R304
1K
C305
.33uF
C306
10uF
Vref
Note: Ground interconnection near audio jacks.

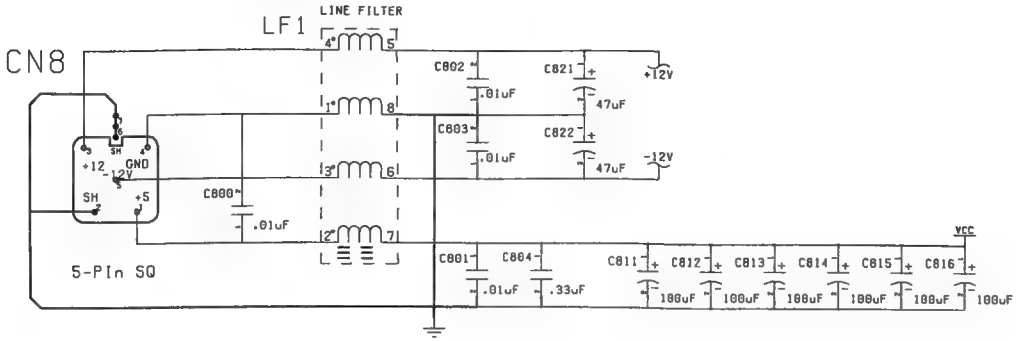

LEFT JOY
CN1
DB9P
RIGHT JOY
CN2
DB9P
CN9
RP401
4.7Kx9
74LS157
U15
U4
8373
DENISE HR
RP405
Note: RP405 Not Used
74HC245
U40
74HC245
U41
HY1
VIDEO
HYBRID
HY1A
COLOR
ANNEX
JP11
VIDEO
DB23S
CN10
RCA JACK
COMPOSITE
Note: R409 Controls Composite output level for 390229-01 Hybrid.
Note: Components designated as Exxx may be loaded with EMI filters, ferrite beads or resistors!
Note: Pin 2 and 21 of HY1 connected internally



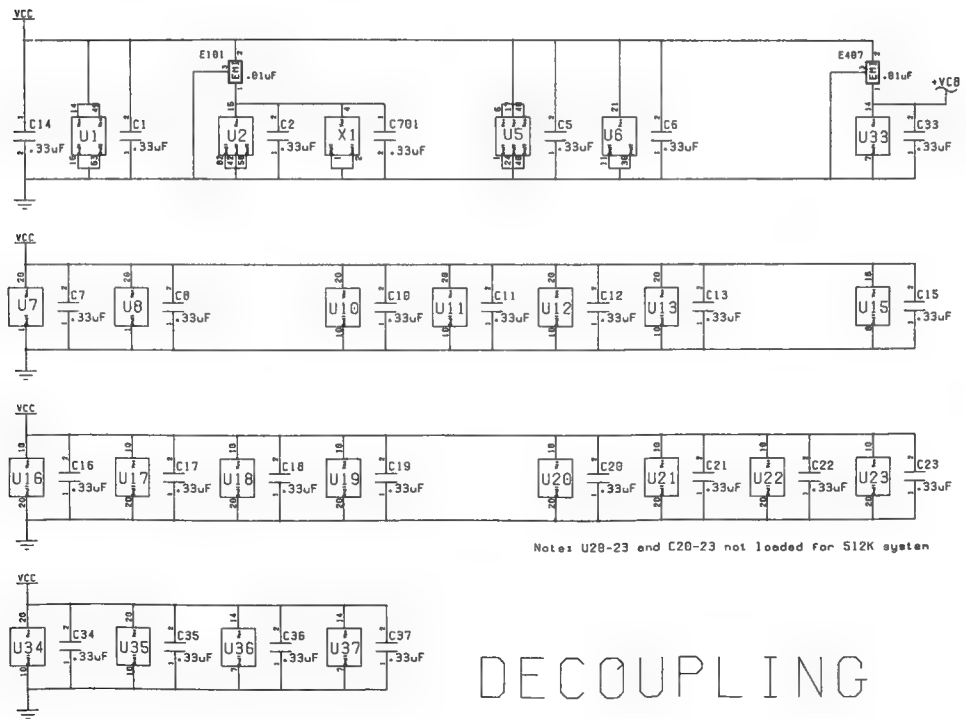
Note: ES01-503 are loaded with 47 Ohm 1/2 W resistors


EXPANSION P1
P1A P1B
JP6
7MHz
CDAC
_OVR
_INT2
_CONFIG
_CCKQ
_CCK
XRDY
_INT6
_FC(2:0)
_IPL(2:0)
_BEER
_VPA
E
_VMA
_RST
_HLT
_BR
_BGACK
_BG
_DTACK
R_W
_LDS
_UDS
_AS
A(23:1)
D(15:0)
XC1
XC2
XC3
47pF
.01uF
E702
E703
E704
-12V
+12V
VCC
DB23S
_RDY
_DKRD
_MTRX
_SEL2
_IORESET
_CHNG
_SIDE
_WPROT
_TRK0
_DKWEB
_DKWDB
_STEP
DIR
_SEL3
_SEL1
_INDEX
100pF
180pF
CN5
EXTERNAL FLOPPY
CN11
CN11 CN11B
_MTRON
_INUSE
_SEL0
_SEL1
_SEL2
_WD
_WE
_RD
_ROY
INTERNAL FLOPPY
U37
74LS32
_RESET
_IORESET
U42
C42
.33uF
R711
R712
1M
47K
C711
C712
.1uF
10uF
NE555
Q711
2N3904
1K
R713
JP1
_KBRESET
C713
POWER UP RESET

POWER INPUT



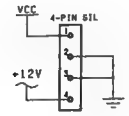
NOTE: HEAVY LINES INDICATE A SINGLE POINT CONNECTION



Note: U20-23 and C20-23 not loaded for 512K system

DECOUPLING

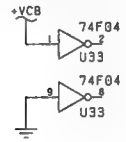
FLOPPY POWER



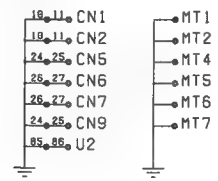
CN12

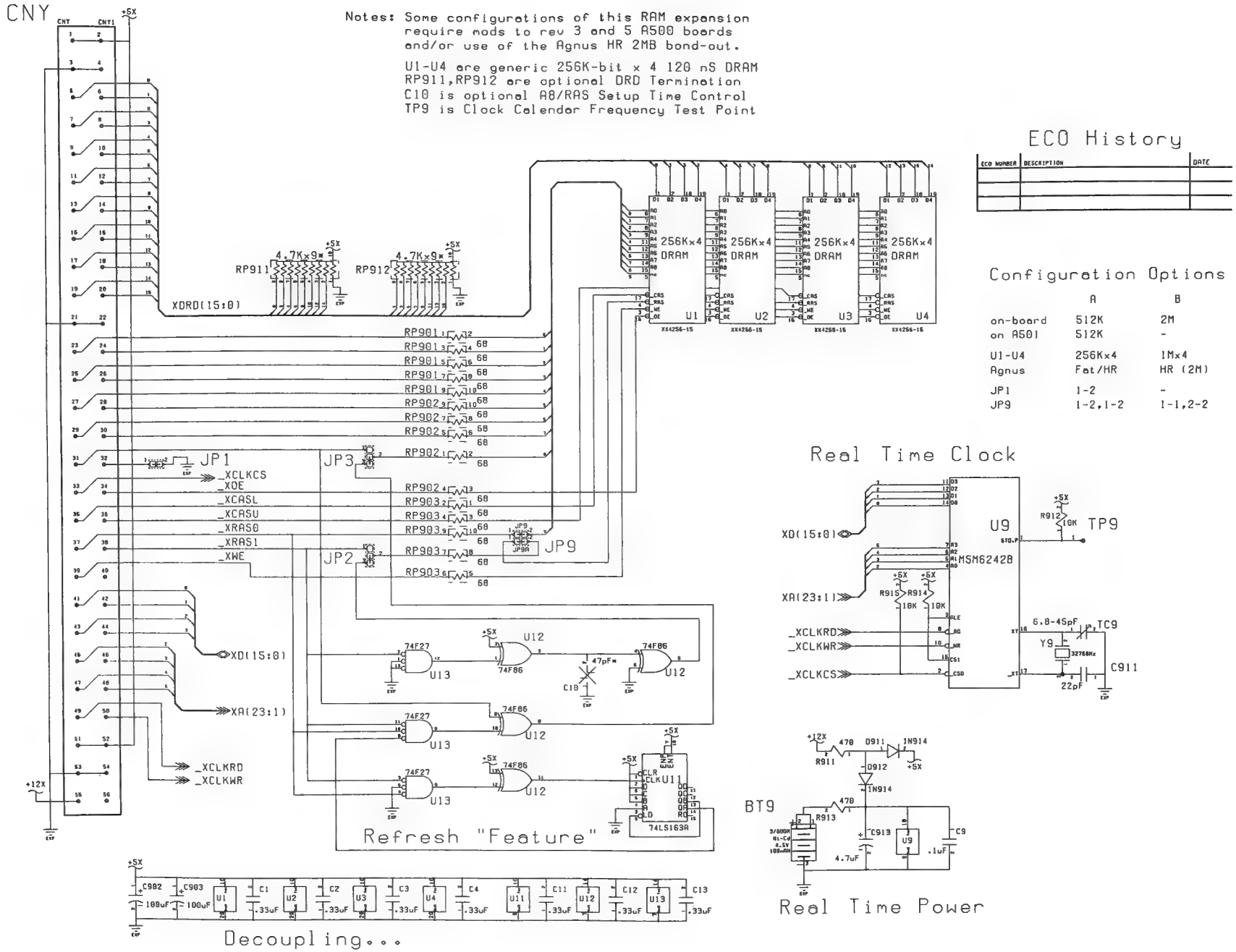
Note: Some drives are +5 only...

SPARES



GROUNDED HOLES, &c.




CNY
Notes: Some configurations of this RAM expansion require mods to rev 3 and 5 A500 boards and/or use of the Agnus HR 2MB bond-out.
U1-U4 are generic 256K-bit x 4 120 nS DRAM
RP911,RP912 are optional DRD Termination
C10 is optional A8/RAS Setup Time Control
TP9 is Clock Calendar Frequency Test Point
ECO History
ECO NUMBER
DESCRIPTION
DATE
Configuration Options
A
B
on-board
512K
2M
on A501
512K
-
U1-U4
256Kx4
1Mx4
Agnus
Fat/HR
HR (2M)
JP1
1-2
-
JP9
1-2,1-2
1-1,2-2
RP911
RP912
4.7Kx9
XDRD(15:0)
256Kx4 DRAM
U1
U2
U3
U4
JP1
JP2
JP3
JP9
_XCLKCS
_XOE
_XCASL
_XCASU
_XRAS0
_XRAS1
_XWE
XD(15:0)
XA(23:1)
_XCLKRD
_XCLKWR
Refresh "Feature"
74F27
74F86
74LS163A
Real Time Clock
MSM62428
TP9
TC9
Y9
C911
Real Time Power
BT9
D911
D912
1N914
C913
Decoupling...
C902
C903
.33uF
100uF

Input/Output Connectors

This section lists pin assignments for several input/output connectors on the Amiga. The information in this section is highly technical and is intended only for those expert in connecting external devices to computers. You do not need this information if you use a cable specifically designed for use with the Amiga and the add-on you want to connect.

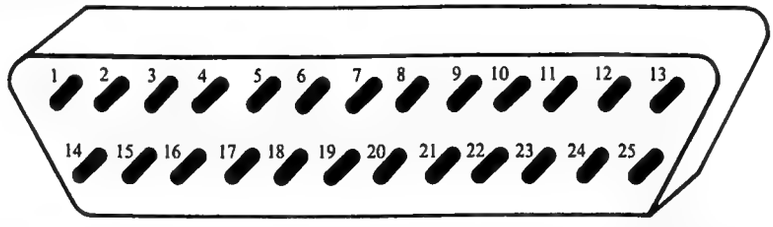
For information about connectors not described in this section, see the *Amiga Hardware Manual*.

If you attach peripherals with cables other than those designed for use with the Amiga, note: **some pins on Amiga connectors provide power outputs and non-standard signals. Attempting to use cables not wired specifically for the Amiga may cause damage to the Amiga or to the equipment you connect.** The descriptions below include specific warnings for each connector. For more information about connecting add-ons, consult your Amiga dealer.

In the descriptions that follow, an asterisk (*) at the end of a signal name indicates a signal that is active low.

Serial Connector

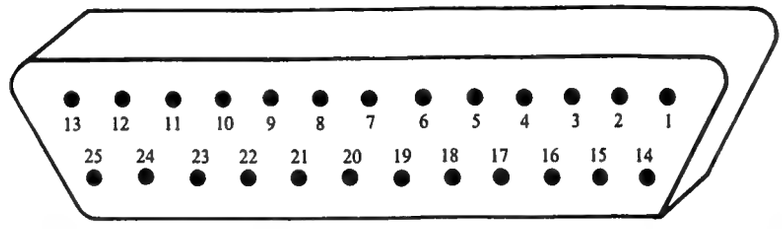
In the following table, the second column from the left gives the Amiga pin assignments. The third and fourth columns from the left give pin assignments for other commonly used connections; the information in these two columns is given for comparison only.



WARNING: Pins 9 and 10 on the Amiga serial connector are used for external power. Connect these pins ONLY if power from them is required by the external device. The table lists the power provided by each of these pins.

Pin	Amiga 500	RS232	HAYES®	Description
1	GND	GND	GND	FRAME GROUND
2	TXD	TXD	TXD	TRANSMIT DATA
3	RXD	RXD	RXD	RECEIVE DATA
4	RTS	RTS		REQUEST TO SEND
5	CTS	CTS	CTS	CLEAR TO SEND
6	DSR	DSR	DSR	DATA SET READY
7	GND	GND	GND	SYSTEM GROUND
8	DCD	DCD	DCD	CARRIER DETECT
9	+12V			+12 VOLT CARRIER
10	−12V			−12 VOLT CARRIER
11	AUDO			AUDIO OUT OF AMIGA
12		S.SD	SI	SPEED INDICATE
13		S.CTS		
14		S.TXD		
15		TXC		
16		S.RXD		
17		RXC		
18	AUDI			AUDIO INTO AMIGA
19		S.RTS		
20	DTR	DTR	DTR	DATA TERMINAL READY
21		SQD		
22	RI	RI	RI	RING INDICATOR
23		SS		
24		TXC1		
25				

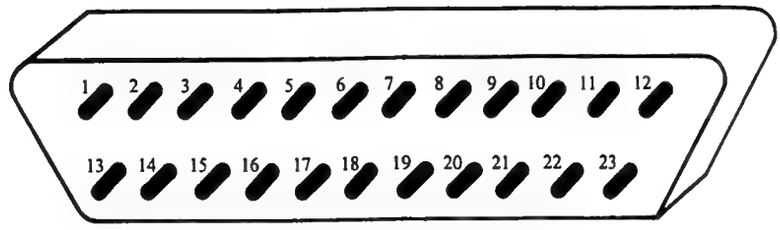
A500 Parallel Connector



WARNING: Pin 14 on the Amiga parallel connector supplies +5 volts of power. Connect this pin ONLY if the power from it is required by the external device. NEVER connect this pin to an output of an external device or to a signal ground. Pins 17-25 are for grounding signals. DO NOT connect these pins directly to a shield ground.

Pin	Name	Description
1	STROBE*	STROBE
2	D0	DATA BIT 0 (Least sign. bit)
3	D1	DATA BIT 1
4	D2	DATA BIT 2
5	D3	DATA BIT 3
6	D4	DATA BIT 4
7	D5	DATA BIT 5
8	D6	DATA BIT 6
9	D7	DATA BIT 7
10	ACK*	ACKNOWLEDGE
11	BUSY	BUSY
12	POUT	PAPER OUT
13	SEL	SELECT
14	+5V PULLUP	+5 VOLTS POWER (100 mA)
15	NC	NO CONNECTION
16	RESET*	RESET
17	GND	SIGNAL GROUND
18	GND	SIGNAL GROUND
19	GND	SIGNAL GROUND
20	GND	SIGNAL GROUND
21	GND	SIGNAL GROUND
22	GND	SIGNAL GROUND
23	GND	SIGNAL GROUND
24	GND	SIGNAL GROUND
25	GND	SIGNAL GROUND

RGB Monitor Connector

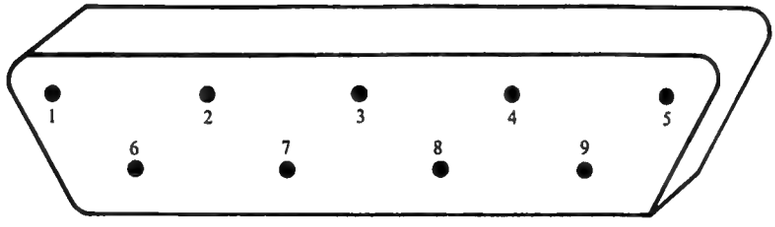


WARNING: Pins 21, 22, and 23 on the RGB monitor connector are used for external power. Connect these pins ONLY if power from them is required by the external device. The table lists the power provided by each of these pins.

Pin	Name	Description
1	XCLK*	EXTERNAL CLOCK
2	XCLKEN*	EXTERNAL CLOCK ENABLE
3	RED	ANALOG RED
4	GREEN	ANALOG GREEN
5	BLUE	ANALOG BLUE
6	DI	DIGITAL INTENSITY
7	DB	DIGITAL BLUE
8	DG	DIGITAL GREEN
9	DR	DIGITAL RED
10	CSYNC*	COMPOSITE SYNC
11	HSYNC*	HORIZONTAL SYNC
12	VSYNC*	VERTICAL SYNC
13	GNDRTN	RETURN FOR XCLKEN*
14	ZD*	ZERO DETECT
15	C1*	CLOCK OUT
16	GND	GROUND
17	GND	GROUND
18	GND	GROUND
19	GND	GROUND
20	GND	GROUND
21	−12V	−12 VOLTS POWER (50 mA)
22	+12V	+12 VOLTS POWER (100 mA)
23	+5V	+5 VOLTS POWER (100 mA)

Mouse/Game Controller Connectors

There are connectors labeled "JOY1" and "JOY2" on the back of the Amiga 500. If you use a mouse to control the Workbench, you must attach it to connector JOY 1. You can attach joystick controllers to either of the connectors. To use a light pen, you must attach it to connector 1. The following tables describe mouse, game controller, and light pen connections.



WARNING: Pin 7 on each of these connectors supplies +5 volts of power. Connect this pin ONLY if power from it is required by the external device.

Connectors 1 and 2: Mouse Connections

Pin	Name	Description
1	MOUSE V	MOUSE VERTICAL
2	MOUSE H	MOUSE HORIZONTAL
3	MOUSE VQ	VERTICAL QUADRATURE
4	MOUSE HQ	HORIZONTAL QUADRATURE
5	MOUSE BUTTON 2	MOUSE BUTTON 2
6	MOUSE BUTTON 1	MOUSE BUTTON 1
7	+5V	+5 VOLTS POWER (100 mA)
8	GND	GROUND
9	MOUSE BUTTON 3	MOUSE BUTTON 3

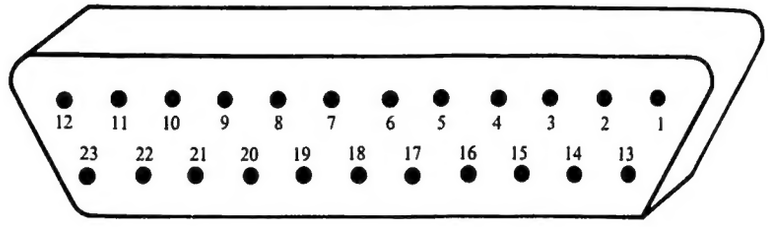
Connectors 1 and 2: Game Controller

Pin	Name	Description
1	FORWARD*	CONTROLLER FORWARD
2	BACK*	CONTROLLER BACK
3	LEFT*	CONTROLLER LEFT
4	RIGHT*	CONTROLLER RIGHT
5	POT X	HORIZONTAL POTENTIOMETER
6	FIRE*	CONTROLLER FIRE
7	+5V	+5 VOLTS POWER (100 mA)
8	GND	GROUND
9	POT Y	VERTICAL POTENTIOMETER

Connector 2: Light Pen Connection

Pin	Name	Description
1		
2		
3		
4		
5	LIGHT PEN PRESS	LIGHT PEN TOUCHED TO SCREEN
6	LIGHT PEN*	CAPTURE BEAM POSITION
7	+5V	+5 VOLTS POWER (100 mA)
8	GND	GROUND
9		

External Disk Connector



Pin	Name	Description
1	/RDY	Disk Ready—Active Low
2	/DKRD	Disk Ready Data—Active Low
3-7	GND	Ground
8	/MTRXD	Disk Motor Control—Active Low
9	/SEL2B	Select Drive 2—Active Low
10	/DRESB	Disk RESET—Active Low
11	/CHNG	Disk has been Removed from Drive—Latched Low
12	+5	5 VDC Supply
13	/SIDEB	Select Disk Side—0 = Upper 1 = Lower
14	/WPRO	Disk is Write Protected—Active Low
15	/TKO	Drive Head Position over Track 0—Active Low
16	/DKWE	Disk Write Enable—Active Low
17	/DKWD	Disk Write Data—Active Low
18	/STEPB	Step the Head—Pulse, First Low then High
19	DIRB	Select Head Direction—0 = Inner 1 = Outer
20	/SEL3B	Select Drive 3—Active Low
21	/SEL1B	Select Drive 1—Active Low
22	/INDEX	Disk Index Pulse—Active Low
23	+12	12 VDC Supply

Power Supply Connector

Pin	Name
1	+5Vdc @ 4.3A
2	SHIELD GROUND
3	+12Vdc @ 1.0A
4	SIGNAL GROUND
5	−12Vdc @ .1A

86-Pin Connector

Pin	Name	Pin	Name
1	gnd	44	IPL2*
2	gnd	45	A16
3	gnd	46	BERR*
4	gnd	47	A17
5	+5	48	VPA*
6	+5	49	gnd
7	exp	50	E
8	−12	51	VMA*
9	exp	52	A18
10	+12	53	RES*
11	exp	54	A19
12	CONFIG*	55	HLT*
13	gnd	56	A20
14	C3*	57	A22
15	CDAC	58	A21
16	C1*	59	A23
17	OVR*	60	BR*
18	XRDY	61	gnd
19	INT2*	62	BGACK*
20	PALOPE*	63	PD15
21	A5	64	BG*
22	INT6*	65	PD14
23	A6	66	DTACK*
24	A4	67	PD13
25	gnd	68	PRW*
26	A3	69	PD12
27	A2	70	LDS*
28	A7	71	PD11
29	A1	72	UDS*
30	A8	73	gnd
31	FC0	74	AS*
32	A9	75	PD0
33	FC1	76	PD10
34	A10	77	PD1
35	FC2	78	PD9
36	A11	79	PD2
37	gnd	80	PD8
38	A12	81	PD3
39	A13	82	PD7
40	IPL0*	83	PD4
41	A14	84	PD6
42	IPL1*	85	gnd
43	A15	86	PD5

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